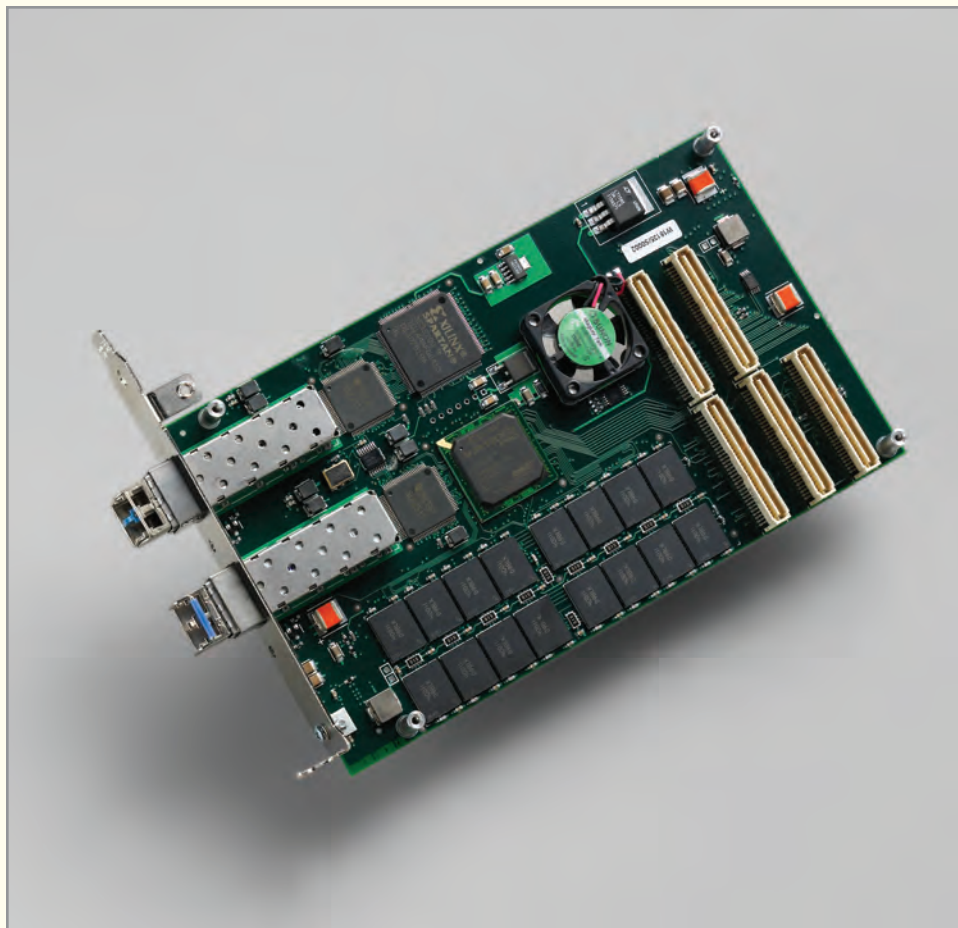


# OCMP

Optical carrier multi-rate interface with programmable oscillators



## Description

The OCMP is a mezzanine board that pairs with a PCI / PCIe main board to support 1GbE (optical or electrical), OC3/12/48 (STM1/4/16), or both.

The dual-channel board has two small form pluggable (SFP) transceivers – one for each channel. Each SFP supports 1GbE (electrical or optical) or OC3/12 (STM1/4), and one supports OC48 (STM16) as well.

Each channel has a programmable Xilinx FPGA (channel 0 has a Virtex II Pro, and channel 1 has a Spartan 3) and a crystal oscillator (XO) for internal reference. The XOs can be programmed independently to any frequency from 10 to 215 MHz.

DRAM (up to 2 GB) is included for snapshot recording and data buffering.

EDT provides FPGA configuration files so you can input and output raw data, detect to a SONET/SDH frame, or descramble a framed signal. Custom configuration files can be requested.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

## Features

Mezzanine board – pairs with an EDT main board (PCI or PCIe), which adds DMA, programmable FPGA resources, and memory

Channel 0: One SFP for 1GbE (optical or electrical) or OC3/12/48 (STM1/4/16), 155.52, 622.08, or 2488.32 Mb/s – 1310 nm

Channel 1: One SFP for the same independent data format options as channel 0, except that OC48 (STM16) can be received but not transmitted

FPGAs: Two programmable (one Xilinx Spartan 3 XC3S200 and one Xilinx Virtex II Pro XC2VP4)

DRAM: Up to 2 GB (DDR) for snapshot recording and data buffering

Clocks: Two XOs (one per channel) for internal reference, each independently programmable from 10 to 215 MHz

## Applications

Telecommunications network monitoring

Ethernet monitoring

SONET/SDH to ethernet conversion

# Specifications

<b>Product Type</b>	OCMP is an optical carrier multi-rate mezzanine board with programmable oscillators; it requires an EDT PCI / PCIe main board.		
<b>FPGA Resources</b>	Two programmable FPGAs (plus FPGA resources on main board): Channel 0 One Xilinx Virtex II Pro XC2VP4 Channel 1 One Xilinx Spartan 3 XC3S200		
<b>Memory</b>	DRAM (DDR) for snapshot recording / data buffering	0 or optional 512 MB or 2 GB; 2 GB is needed for snapshot recording at rates of OC48/STM16 or faster with PCI SS or PCI GS main board	
<b>Clocks</b>	Two XOs (one per channel, for internal reference)	Either can be programmed to any frequency from 10 to 215 MHz	
<b>Data Rates</b>	Dependent on such factors as data format, main board, and system variables.		
<b>Data Format (I/O)</b>	Channel 0 Channel 1	1GbE (1000 Base-T or -X) or SONET OC3/12/48 (SDH STM1/4/16) Same options as for channel 0, or optional OC3/12 (STM1/4)	
<b>Transceivers</b>	Two (channels 0 and 1 each have one) are included, supporting data as shown below.		
	<b>CHANNEL 0 (1 SFP, included)</b>	<b>ELECTRICAL 1GbE</b>	<b>OPTICAL 1GbE or OC3/12/48 (STM1/4/16) 1310 nm</b>
	Output power	–	–9.5 to –3 dBm
	Center wavelength	–	1270 to 1360 nm
	Sensitivity	–	–18 dBm
	Maximum input power	–	0 dBm
	Connector	RJ45	LC
	<b>CHANNEL 1 (1 SFP, included)</b>	<b>1GbE</b>	<b>1GbE or OC3/12/48 (STM1/4/16) 1310 nm</b>
	Output power	–	–9.5 to –3 dBm
	Center wavelength	–	1270 to 1360 nm
	Sensitivity	–	–18 dBm
	Maximum input power	–	0 dBm
	Connector	RJ45	LC
<b>Connectors</b>	One RJ45 or LC on each transceiver as shown above.		
<b>Cabling</b>	Consult EDT for purchase options.		
<b>Physical</b>	Weight	3.5 oz. typical	
	Dimensions	6.6 x 4.2 x 0.75 in. (with a main board)	
<b>Environmental</b>	Temperature	Operating 0° to 40° C Non-operating –40° to 70° C	
	Humidity	Operating 1% to 90%, non-condensing at 40° C Non-operating 95%, non-condensing at 45° C	
<b>System and Software</b>	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board		

## Ordering Options

- Main board: PCI SS / PCI GS / PCIe8 LX
- DRAM: **0** / 512 MB / 2 GB
- Transceivers: 2 [options above]

**Bold** is default. For more options, see main board detail. **Ask** about custom options.