

DRX16

Dual receiver with 16-bit analog-to-digital converters (ADCs)



Description

The DRX16 is a mezzanine board that pairs with a PCIe main board to receive two intermediate frequency (IF) signals simultaneously.

The board has a configurable Xilinx Virtex 6 LX FPGA (XC6VLX240T) and two identical IF input channels. Each channel provides one IF direct module (IDX) that supports any frequency from DC to 300 MHz.

The gain option, which must be the same on both channels, can be no gain (option A); programmable on the board (option B); or programmable on the board and fixed on the IDX modules (option C).

For option A, each module's output is digitized by a 16-bit ADC and captured in the FPGA. For options B and C, each module's output is amplified with a PGA before being digitized by the ADC and captured in the FPGA. The FPGA can perform signal processing or route data to the main board.

Each channel has a sample clock that can be tuned from 10 to 200 MHz. A third clock is available via the sample clock I/O connector, which can be set as input or output.

For the timebase, you can use the 10 MHz TCXO provided, or connect your own source via the reference input. A reference output and a time code input (1 pps or IRIG-B) also are included.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Features

Mezzanine board – pairs with an EDT main board (PCIe8 LX / FX), which adds DMA, programmable FPGA resources, and memory

FPGA: One programmable Xilinx Virtex 6 (XC6VLX240T)

Channels: Two identical– each with one IF direct module (IDX) that supports DC to 300 MHz, with three gain options:

- Option A = no gain
- Option B = programmable gain on board
- Option C = programmable gain on board plus fixed gain on IDX modules

ADCs: Two 16-bit (one per channel)

Sample clock: Independently programmable for each channel (10 to 200 MHz)

Sample clock I/O: Programmable as input or output

Timebase: 10 MHz TCXO or reference input, available via reference output

Time code: 1 pps or IRIG-B input

Applications

IF receiver

Software-defined radio

Surveillance / spectrum monitoring

Digital tuning

Test and measurement

Specifications

Product Type	DRX16 is a dual receiver mezzanine board for IF; it requires an EDT PCIe main board.																																		
FPGAs and Memory	One programmable FPGA (Xilinx Virtex 6 LX (XC6VLX240T), plus FPGA and memory resources on main board																																		
Sample Clock	User-configurable & phase-locked to timebase	Tuning range = 10 to 200 MHz (independently programmable for each channel)																																	
ADCs (one per channel)	Resolution / maximum sample rate	16 bits / 200 MHz																																	
Data Rates	Dependent on such factors as data format, main board, and system variables.																																		
Data Format (I/O)	<p>Two identical user-configurable IF channel inputs, each supporting one user-configurable IF direct module (IDX) One time code input from external receiver (1 pps or IRIG-B, with user-configurable output) One reference input (for user-supplied timebase, if desired) One reference output One sample clock I/O (can be programmed to be either input or output)</p> <p>As shown below, the gain option (A, B, or C) must be the same for both identical IF channels (0 & 1), each with its IDX module.</p> <table border="1"> <thead> <tr> <th>TWO IDENTICAL IF CHANNELS (0 & 1)</th> <th>Option A: Both DRX16 IDX</th> <th>Option B: Both DRX16-PG IDX</th> <th>Option C: Both DRX16-PG IDX-FG</th> </tr> </thead> <tbody> <tr> <td>Gain</td> <td>None (no gain)</td> <td>Programmable on board</td> <td>Programmable on board; fixed on IDX modules</td> </tr> <tr> <td>Frequency range</td> <td>DC to 300 MHz</td> <td>*</td> <td>*</td> </tr> <tr> <td>-3 dB bandwidth</td> <td>300 MHz</td> <td>*</td> <td>*</td> </tr> <tr> <td>Input impedance</td> <td>50 or optional 75 Ω</td> <td>*</td> <td>*</td> </tr> <tr> <td>Return loss</td> <td>16 dB</td> <td>*</td> <td>*</td> </tr> <tr> <td>Signal level</td> <td>+15 dBm (max)</td> <td>-12 to +6 dBm</td> <td>-55 to -10 dBm</td> </tr> <tr> <td>Typical SNR / SFDR</td> <td>70 / 75 dB</td> <td>70 / 60 dB</td> <td>Max gain 55 / 45 dB; min gain 70 / 60 dB</td> </tr> </tbody> </table> <p>* This specification is the same for all three gain options (A, B, and C).</p>			TWO IDENTICAL IF CHANNELS (0 & 1)	Option A: Both DRX16 IDX	Option B: Both DRX16-PG IDX	Option C: Both DRX16-PG IDX-FG	Gain	None (no gain)	Programmable on board	Programmable on board; fixed on IDX modules	Frequency range	DC to 300 MHz	*	*	-3 dB bandwidth	300 MHz	*	*	Input impedance	50 or optional 75 Ω	*	*	Return loss	16 dB	*	*	Signal level	+15 dBm (max)	-12 to +6 dBm	-55 to -10 dBm	Typical SNR / SFDR	70 / 75 dB	70 / 60 dB	Max gain 55 / 45 dB; min gain 70 / 60 dB
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Timebase	10 MHz TCXO	Reference input	Reference output																																
Frequency tolerance	+/- 0.5 ppm at 25° C	–	–																																
Frequency over temperature	+/- 2.5 ppm at 0° to 75° C	–	–																																
Impedance	–	50 Ω	50 Ω																																
Signal level	–	0 to 7 usable (11 max) dBm	2 V peak to peak (ptp)																																
Return loss	–	12 dB	–																																
Connectors	Both IF inputs = SMB 50 or optional 75 Ω; sample clock I/O and both reference connectors = SMB 50 Ω; time code input = 7-pin Lemo																																		
Cabling	Consult EDT for purchase options: To 7-pin Lemo on board, from time code source	Via one DB9 (for 1 pps or IRIG-B) or BNC (for IRIG-B only)																																	
Physical	Weight	5.6 oz. typical																																	
	Dimensions	6.6" L x 4.2" W x 0.5" H (with a main board)																																	
Environmental	Temperature	Operating 0° to 40° C Non-operating -40° to 70° C																																	
	Humidity	Operating 1% to 90%, non-condensing at 40° C Non-operating 95%, non-condensing at 45° C																																	
System and Software	For details on system requirements and EDT-provided software driver packages, see specifications for your EDT main board.																																		

Ordering Options

Main board: PCIe8 LX / FX (required)
 Gain: Option **A** / B / C (details above)
 Connectors (for IF inputs): **50** / 75 Ω
 Cabling (for time code input, if any): DB9 / BNC

Bold is default. For more options, see main board detail. **Ask** about custom options.