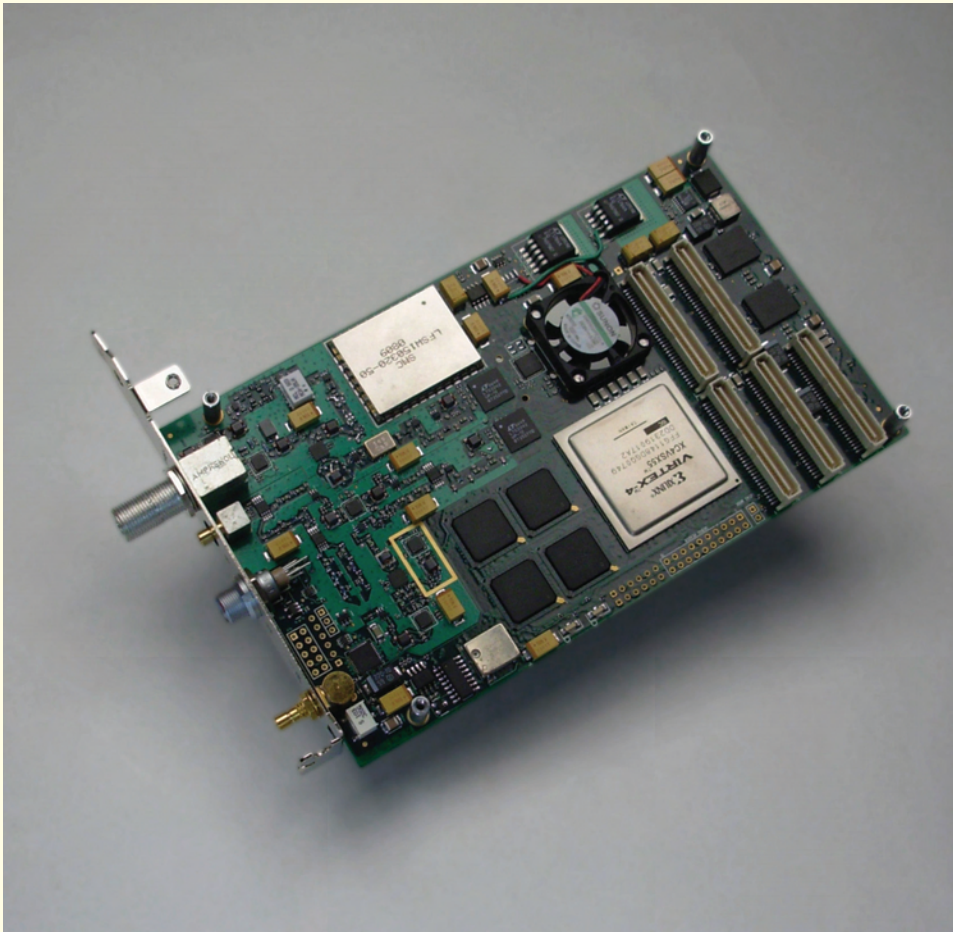


SRXL2

Signal receiver and processor for L-band and IF – v. 2



Description

The SRXL2 is a mezzanine board that pairs with an EDT main board (for PCI or PCI Express) to receive and process two simultaneous RF inputs.

Sampling rates depend upon the module used: IF direct module (IDM), IF mixer module (IMM), or L-band module (LBM). Channel 0 supports either of the first two, while channel 1 supports any of the three modules.

IDM supports any frequency over 10 MHz that meets Nyquist criteria. A 90-MHz lowpass filter is optional.

IMM supports 140 or 160 MHz input, mixed to 55 MHz (center). Bandpass filtering, not provided, is performed externally.

LBM supports 900 to 2250 MHz input, mixed to 187.5 MHz (center) with 500 kHz tuning resolution; bandwidth is 116 MHz.

Module outputs are digitized with 12-bit precision ADCs and captured in the programmable Xilinx Virtex 4 SX FPGA. The FPGA can perform signal processing or serve as a configurable switch matrix to route data to the main board and four digital down-converter Graychips (GC4016).

A 10 MHz TCXO is provided, or you can connect your own reference clock. A 1 pps or IRIG-B time code input also is included.

The main board supplies DMA, plus additional memory and programmable FPGA resources.

Applications

- Satellite receiver
- Software-defined radio
- Surveillance / spectrum monitoring
- Digital tuning
- Test and measurement equipment

Features

Mezzanine board – pairs with an EDT main board (in a PCI, PCI-X, or PCIe bus), which adds DMA, programmable FPGA resources, and memory

Two configurable RF channels (0 and 1) with simultaneous 12-bit ADC

Channel 0 - supports IF direct module (IDM) or IF mixer module (IMM):

- IDM supports input over 10 MHz, with optional 90-MHz lowpass filter
- IMM supports input of 140 or 160 MHz, mixed to 55 MHz (center); bandwidth is determined by external filtering (not provided)

Channel 1 - supports either module above, or L-band module (LBM) for input of 900 to 2250 MHz, mixed to 55 MHz (center), with 500 kHz tuning resolution; bandwidth is 116 MHz

FPGA: One programmable Xilinx Virtex 4 SX XC4VSX55

Graychips: Four optional (TI GC4016) for 16-channel digital down-conversion

Sample clock: Programmable to any frequency from 10 to 250 MHz

Reference clock: Onboard 10 MHz TCXO or external reference input

Time code: 1 pps, IRIG-B, or other input, with user-configurable output

Specifications

Product Type	SRXL2 is a signal receiver mezzanine board (v. 2) for L-band and IF; it requires a main board.			
FPGAs and Memory	One programmable FPGA (Xilinx Virtex 4 SX XC4VSX55), plus FPGA and memory resources on main board			
Graychips	Four programmable (TI GC4016) for digital down-conversion			
Sample Clock and Converter (A/D)	Sample clock tuning range	10-250 MHz, programmed through FPGA and phase-locked to 10-MHz reference		
	Converter resolution / maximum sample rate	12 bits / 250 MHz		
Data Rates	Data rates are dependent on data format and main board.			
Data Format (I/O)	Inputs: One time code, one external reference, and two configurable data inputs, as shown below.			
	Time code (from external receiver): 1 pps, IRIG-B, or other input, with user-configurable output			
	Reference - 10 MHz external: Input impedance is 50 Ω ; return loss is 12 dB; signal level is 0 to 7 dBm usable (11 dBm maximum)			
	CHANNEL 0	IDM: IF direct module	IMM: IF mixer module	
	Frequency range / center	10 MHz minimum / None	140 or 160 MHz / 55 MHz	
	-3 dB bandwidth	Determined externally	Determined externally	
	Filter options	90 MHz lowpass filter	n/a	
	Input impedance	75 or optional 50 Ω	75 or optional 50 Ω	
	Return loss	16 dB	16 dB	
	Signal level (usable / max)	-65 to -20 / 0 dBm	-65 to -20 / 0 dBm	
	Typical SNR / SFDR	TBD (dB)	TBD (dB)	
	CHANNEL 1	IDM: IF direct module	IMM: IF mixer module	LBM: L-band module
	Frequency range / center	10 MHz minimum / None	140 or 160 MHz / 55 MHz	900 to 2250 MHz / 187.5 MHz
	-3 dB bandwidth	Determined externally	Determined externally	116 MHz
	Filter options	90 MHz lowpass filter	n/a	n/a
	Input impedance	75 or optional 50 Ω	75 or optional 50 Ω	75 Ω
	Return loss	16 dB	16 dB	16 dB
	Signal level (usable / max)	-65 to -20 / 0 dBm	-65 to -20 / 0 dBm	65 to -20 / 0 dBm
	Typical SNR / SFDR	TBD (dB)	TBD (dB)	TBD (dB)
Local Oscillators		IDM	IMM	LBM (oscillator 1)
	Tuning range	n/a	215 or 195 MHz (fixed)	1700-2950 MHz
	Tuning step size	n/a	n/a	500 kHz
				LBM (oscillator 2)
				562.5 MHz (fixed)
				n/a
Reference - 10 MHz TCXO	Adjustment range +/- 3 ppm; frequency tolerance +/- 0.5 ppm at 25° C; frequency over temperature +/- 2.5 ppm at 0° to 75° C			
Connectors	For time code, 7-pin Lemo; for external reference, SMB 50 Ω ; for IDM and IMM modules, SMB 50 or 75 Ω ; for LBM module, F-type 75 Ω			
Cabling	Consult EDT for purchase options:			
	To 7-pin Lemo on board, from time code source	Via one DB9 (for 1 pps or IRIG-B) or BNC (for IRIG-B only)		
Physical	Weight	4.9 oz. typical		
	Dimensions	6.6 x 4.2 x 0.5 in. (with a main board)		
Environmental	Temperature	Operating 0° to 40° C Non-operating -40° to 70° C		
	Humidity	Operating 1% to 90% (non-condensing at 40° C) Non-operating 95% (non-condensing at 45° C)		
System and Software	System requirements and EDT-provided software driver packages are discussed in the specifications for your EDT main board.			

Support

EDT offers engineer-to-engineer customer support, from phone consultation to custom design of hardware, firmware, and software. Contact us for options and details.

Contact

Engineering Design Team (EDT), Inc.
1400 NW Compton Drive, Suite 315
Beaverton, Oregon 97006
800-435-4320 / 503-690-1234 (phone)
503-690-1243 (fax)
www.edt.com

Ordering Options

- Main board: PCI GS / PCIe8 LX
- Graychips: 0 / 4
- Channels 0 and 1: IDM / IMM / LBM (on 1 only)
- Connectors: 50 / 75 Ω (IF)
- Cabling (for time code input): DB9 / BNC

Bold is default. For more options, see main board datasheet. **Ask about custom options.**