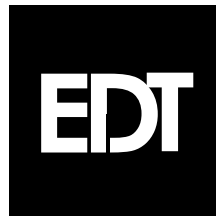


PCI DV

PCI Bus Digital Video Board
Addendum for

Generic AIA Digital Camera Interface

008-00983-02



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Overview

The PCI Bus Digital Video Camera Interface is a single-slot PCI Bus board that implements a high-speed DMA channel between an external digital video camera and a host computer. The device interface side of the board consists of thirty-five RS-422-compatible driver/receivers connected to a Xilinx RAM-based programmable gate array. These driver/receivers can be assigned as inputs or outputs in groups of four. The Xilinx device can be programmed to implement arbitrary interface protocols by executing a program that downloads a bit pattern from a file to the PCI DV board.

Some versions of the firmware allow you to enable a *region of interest*, a rectangle you can define to crop an image horizontally and vertically, thus eliminating superfluous pixels.

This document describes the PCI DV firmware for a wide range of digital cameras that send 16 data bits or fewer per video clock cycle. Many of these cameras follow the specification for AIA Monochrome Digital Cameras (see “References” on page 21 for the complete specification reference). To handle variations among cameras, EDT provides special cables, programmable registers, and in some cases special Xilinx firmware configuration files.

For further information on using the PCI Bus Digital Video Camera Interface, contact EDT and ask for the *PCI DV User’s Guide* (part number 008-00966).

Included Files

The following files are shipped with the PCI DV for generic AIA cameras (others may be available to support other cameras). The appropriate file is loaded when you choose your camera model, using the configuration program *camconfig* or *initcam*, provided with the PCI DV software.

camera_config/aiag.bitfirmware for generic AIA monochrome digital cameras

camera_config/aiagce.bitfirmware for Cinnacinnati Electronics digital cameras

Serial Communications Protocol

The serial control lines are fixed at 8 data bits, one stop bit, no parity. The default baud rate is 9600 baud; you can change this using the Serial Data Control register (described on page 13).

Connector Pinout

The PCI Bus Digital Video Camera Interface uses a high-density 80-pin I/O connector. Many digital cameras use a 68-pin female high-density connector that follows the *AIA Monochrome Digital Camera with Category I Extended Interface* specification. EDT can provide appropriate cables that adapt the PCI DV board to these or other cameras.

The 68-pin male cable connector used with many of these cameras is AMP part number 749621-7, with a shielded backshell (AMP part number 750752-1).

The following pinout diagrams describe the connection from the cable to these cameras. The connection from the PCI DV board to the cable is described in the *PCI DV User's Guide* (part number 008-00966), available from Engineering Design Team, Inc.

AIA Pin	AIA Signal	PCI DVK Signal	AIA Pin	AIA Signal	PCI DVK Signal
1	Ground	Ground	35	Ground	Ground
2	MSB+	VD0 +	36	MSB –	VD0 –
3	MSB-1 +	VD1 +	37	MSB-1 –	VD1 –
4	MSB-2 +	VD2 +	38	MSB-2 –	VD2 –
5	MSB-3 +	VD3 +	39	MSB-3 –	VD3 –
6	MSB-4 +	VD4 +	40	MSB-4 –	VD4 –
7	MSB-5 +	VD5 +	41	MSB-5 –	VD5 –
8	MSB-6 +	VD6 +	42	MSB-6 –	VD6 –
9	MSB-7 +	VD7 +	43	MSB-7 –	VD7 –
10	MSB-8 +	VD8 +	44	MSB-8 –	VD8 –
11	MSB-9 +	VD9 +	45	MSB-9 –	VD9 –
12	Ground	Ground	46	Ground	Ground
13	MSB-10 +	VD10 +	47	MSB-10 –	VD10 –
14	MSB-11 +	VD11 +	48	MSB-11 –	VD11 –
15	MSB-12 +	VD12 +	49	MSB-12 –	VD12 –
16	MSB-13 +	VD13 +	50	MSB-13 –	VD13 –
17	do not use		51	do not use	
18	do not use		52	do not use	
19	MSB-14 +	VD14 +	53	MSB-14 –	VD14 –
20	MSB-15 +	VD15 +	54	MSB-15 –	VD15 –
21	reserved		55	reserved	
22	Serial Control Out +	SCNTLO +	56	Serial Control Out –	SCNTLO –
23	Serial Cont. In +	SCNTLI +	57	Serial Cont. In –	SCNTLI –
24	Field ID +	FLDID +	58	Field ID –	FLDID –
25	Frame Enable +	FRME +	59	Frame Enable –	FRME –
26	Line Enable +	LINE +	60	Line Enable –	LINE –
27	Channel ID 0 +	ID0 +	61	Channel ID 0 –	ID0 –
28	Channel ID 1 +	ID1 +	62	Channel ID 1 –	ID1 –
29	Pixel Data Strobe +	PSTRB +	63	Pixel Data Strobe –	PSTRB –
30	Mode Control 0 +	FRMRST / EXP +	64	Mode Control 0 –	FRMRST / EXP –
31	Mode Control 1 +	MC0 +	65	Mode Control 1 –	MC0 –
32	Mode Control 2 +	MC1 +	66	Mode Control 2 –	MC1 –
33	Mode Control 3 +	MC2 +	67	Mode Control 3 –	MC2 –
34	Ground	Ground	68	Ground	Ground

Table 1. PCI DVK for Single-channel Grayscale Cameras

AIA Pin	AIA Signal	PCI DVK Signal	AIA Pin	AIA Signal	PCI DVK Signal
1	ground	ground	35	ground	ground
2	AMSB+	VDA0+	36	AMSB-	VDA0-
3	AMSB-1 +	VDA1+	37	AMSB-1 -	VDA1-
4	AMSB-2 +	VDA2+	38	AMSB-2-	VDA2-
5	AMSB-3 +	VDA3+	39	AMSB-3-	VDA3-
6	AMSB-4 +	VDA4+	40	AMSB-4 -	VDA4-
7	AMSB-5 +	VDA5+	41	AMSB-5-	VDA5-
8	AMSB-6 +	VDA6+	42	AMSB-6-	VDA6-
9	AMSB-7 +	VDA7+	43	AMSB-7 -	VDA7-
10	BMSB +	VDB0+	44	BMSB-	VDB0-
11	BMSB-1 +	VDB1+	45	BMSB-1 -	VDB1-
12	ground	ground	46	ground	ground
13	BMSB-2 +	VDB2+	47	BMSB-2-	VDB2-
14	BMSB-3 +	VDB3+	48	BMSB-3 -	VDB3-
15	BMSB-4 +	VDB4+	49	BMSB-4-	VDB4-
16	BMSB-5 +	VDB5+	50	BMSB-5 -	VDB5-
17	do not use		51	do not use	
18	do not use		52	do not use	
19	BMSB-6 +	VDB6+	53	BMSB-6 -	VDB6-
20	BMSB-7 +	VDB7+	54	BMSB-7 -	VDB7-
21	AMSB-8+	VDA8+	55	AMSB-8-	VDA8-
22	Serial Control Out +	SCNTLO+	56	Serial Control Out -	SCNTLO-
23	Serial Cont. In +	SCNTLI+	57	Serial Cont. In -	SCNTLI-
24	Field ID +	FLDID+	58	Field ID -	FLDID-
25	Frame Enable +	FRME+	59	Frame Enable -	FRME-
26	Line Enable +	LINE+	60	Line Enable-	LINE-
27	Channel ID 0 +	ID0+	61	Channel ID 0 -	ID0-
28	Channel ID 1 +	ID1+	62	Channel ID 1 -	ID1-
29	Pixel Data Strobe +	PSTRB+	63	Pixel Data Strobe -	PSTRB-
30	EXPOSE +	EXPOSE+	64	EXPOSE -	EXPOSE-
31	AMSB-9 +	VDA9+	65	AMSB-9 -	VDA9-
32	BMSB-8+	VDB8+	66	BMSB-8 -	VDB8-
33	BMSB-9+	VDB9+	67	BMSB-9-	VDB9-
34	ground	ground	68	ground	ground

Table 2. PCI DVK for Dual-channel Grayscale Cameras

AIA Pin	AIA Signal	PCI DV Signal	AIA Pin	AIA Signal	PCI DV Signal
1	ground	ground	41	ground	ground
2	not used		42	not used	
3	MSB4+	VD4+	43	MSB0+	VD0+
4	MSB4-	VD4-	44	MSB0-	VD0-
5	MSB5+	VD5+	45	MSB1+	VD1+
6	MSB5-	VD5-	46	MSB1-	VD1-
7	MSB6+	VD6+	47	MSB2+	VD2+
8	MSB6-	VD6-	48	MSB2-	VD2-
9	MSB7+	VD7+	49	MSB3+	VD3+
10	MSB7-	VD7-	50	MSB3-	VD3-
11	MSB12+	VD12+	51	MSB8+	VD8+
12	MSB12-	VD12-	52	MSB8-	VD8-
13	MSB13+	VD13+	53	MSB9+	VD9+
14	MSB13-	VD13-	54	MSB9-	VD9-
15	MSB14+	VD14+	55	MSB10+	VD10+
16	MSB14-	VD14-	56	MSB10-	VD10-
17	MSB15+	VD15+	57	MSB11+	VD11+
18	MSB15-	VD15-	58	MSB11-	VD11-
19	not used		59	not used	
20	+5V	+5V	60	+5V	+5V
21	not used		61	not used	
22	not used		62	not used	
23	not used		63	not used	
24	Serial Control Line In+	SCNTLI +	64	Pixel Strobe +	PSTRB+
25	Serial Control Line In-	SCNTLI -	65	Pixel Strobe -	PSTRB -
26	Channel ID 0+	ID0+	66	LineEnable+	LINE +
27	Channel ID 0-	ID0-	67	Line Enable-	LINE -
28	Channel ID 1+	ID1+	68	Frame Enable+	FRME +
29	Channel ID 1-	ID1-	69	Frame Enable-	FRME -
30	not used		70	Field ID+	FLDID +
31	not used		71	Field ID-	FLDID -
32	Serial Control Line Out +	SCNTLO+	72	Mode Control 0	MC0
33	Serial Control Line Out -	SCNTLO-	73	not used	
34	not used		74	Mode Control 1	MC1
35	not used		75	not used	
36	not used		76	Mode Control 2	MC2
37	not used		77	not used	
38	not used		78	FRMRST/EXP+	EXPOSE+
39	not used		79	FRMRST/EXP-	EXPOSE -
40	Ground		80	Ground	

Table 3. PCI DV for Single-channel Grayscale Cameras

AIA Pin	AIA Signal	PCI DV Signal	AIA Pin	AIA Signal	PCI DV Signal
1	do not use	do not use	41	do not use	do not use
2	do not use	do not use	42	do not use	do not use
3	AMSB-4 +	VDA4+	43	AMSB +	VDA0+
4	AMSB-4-	VDA4-	44	AMSB -	VDA0-
5	AMSB-5 +	VDA5+	45	AMSB-1+	VDA1+
6	AMSB-5 -	VDA5-	46	AMSB-1 -	VDA1-
7	AMSB-6 +	VDA6+	47	AMSB-2+	VDA2+
8	AMSB-6 -	VDA6-	48	AMSB-2 -	VDA2-
9	AMSB-7+	VDA7+	49	AMSB-3+	VDA3+
10	AMSB-7 -	VDA7-	50	AMSB-3 -	VDA3-
11	BMSB-4+	VDB4+	51	BMSB +	VDB0+
12	BMSB-4-	VDB4-	52	BMSB -	VDB0-
13	BMSB-5+	VDB5+	53	BMSB-1+	VDB1+
14	BMSB-5-	VDB5-	54	BMSB-1 -	VDB1-
15	BMSB-6+	VDB6+	55	BMSB-2+	VDB2+
16	BMSB-6-	VDB6-	56	BMSB-2 -	VDB2-
17	BMSB-7+	VDB7+	57	BMSB-3+	VDB3+
18	BMSB-7-	VDB7-	58	BMSB-3-	VDB3-
19	AMSB-8 +	VDA8+	59	AMSB-8 -	VDB8-
20	+5 V	+5 V	60	+5 V	+5 V
21	AMSB10+	VDA10+	61	AMSB-10-	VDA10-
22	AMSB11+	VDA11+	62	AMSB-11-	VDA11-
23	ground	ground	63	ground	ground
24	Serial Control In +	SCNTLI+	64	pixel data strobe +	PSTRB+
25	Serial Control In -	SCNTLI-	65	pixel data strobe -	PSTRB -
26	BMSB-10+	VDB10+	66	line enable +	LINE +
27	BMSB-10-	VDB10-	67	line enable -	LINE -
28	Bloomflag +	reserved	68	frame enable +	FRME +
29	Bloomflag -	reserved	69	frame enable -	FRME -
30	TRIG +	reserved	70	BMSB-11+	VDB11+
31	TRIG -	reserved	71	BMSB-11-	VDB11-
32	Serial Control Out +	SCNTLO+	72	AMSB-9+	VDA9+
33	Serial Control Out -	SCNTLO-	73	AMSB-9-	VDA9-
34	do not use	do not use	74	BMSB-8+	VDB8+
35	do not use	do not use	75	BMSB-8-	VDB8-
36	do not use	do not use	76	BMSB-9+	VDB9+
37	do not use	do not use	77	BMSB-9-	VDB9-
38	FRMRST/EXP +	EXPOSE+	78	do not use	do not use
39	FRMRST/EXP -	EXPOSE-	79	do not use	do not use
40	ground	ground	80	ground	ground

Table 4. PCI DV for Dual-channel Grayscale Cameras

AIA Pin	AIA Signal	PCI DVK Signal	AIA Pin	AIA Signal	PCI DVK Signal
1	ground	ground	35	ground	ground
2	RedMSB-0+	VDR0+	36	RedMSB-0-	VDR0-
3	RedMSB-1 +	VDR1+	37	RedMSB-1 -	VDR1-
4	RedMSB-2 +	VDR2+	38	RedMSB-2-	VDR2-
5	RedMSB-3 +	VDR3+	39	RedMSB-3-	VDR3-
6	RedMSB-4 +	VDR4+	40	RedMSB-4 -	VDR4-
7	RedMSB-5 +	VDR5+	41	RedMSB-5-	VDR5-
8	RedMSB-6 +	VDR6+	42	RedMSB-6-	VDR6-
9	RedMSB-7 +	VDR7+	43	RedMSB-7 -	VDR7-
10	GrnMSB -0+	VDG0+	44	GrnMSB-0-	VDG0-
11	GrnMSB-1 +	VDG1+	45	GrnMSB-1 -	VDG1-
12	ground	ground	46	ground	ground
13	GrnMSB-2 +	VDG2+	47	GrnMSB-2-	VDG2-
14	GrnMSB-3 +	VDG3+	48	GrnMSB-3 -	VDG3-
15	GrnMSB-4 +	VDG4+	49	GrnMSB-4-	VDG4-
16	GrnMSB-5 +	VDG5+	50	GrnMSB-5 -	VDG5-
17	do not use		51	do not use	
18	BluMSB-4+	VDB4+	52	BluMSB-4-	VDB4-
19	GrnMSB-6 +	VDG6+	53	GrnMSB-6 -	VDG6-
20	GrnMSB-7 +	VDG7+	54	GrnMSB-7 -	VDG7-
21	BluMSB-0+	VDB0+	55	BluMSB-0-	VDB8-
22	Serial Control Out +	SCNTLO+	56	Serial Control Out -	SCNTLO-
23	Serial Cont. In +	SCNTLI+	57	Serial Cont. In -	SCNTLI-
24	BluMSB-5+	VDB5+	58	BluMSB-5 -	VDB5-
25	Frame Enable +	FRME+	59	Frame Enable -	FRME-
26	Line Enable +	LINE+	60	Line Enable-	LINE-
27	BluMSB-6+	VDB6+	61	BluMSB-6-	VDB6-
28	BluMSB-7+	VDB7+	62	BluMSB-7 -	VDB7-
29	Pixel Data Strobe +	PSTRB+	63	Pixel Data Strobe -	PSTRB-
30	EXPOSE +	EXPOSE+	64	EXPOSE -	EXPOSE-
31	BluMSB-1+	VDB1+	65	BluMSB-1 -	VDB1-
32	BluMSB-2+	VDB2+	66	BluMSB-2 -	VDB2-
33	BluMSB-3+	VDB3+	67	BluMSB-3-	VDB3-
34	ground	ground	68	ground	ground

Table 5. PCI DVK for Single-channel Color Cameras

Xilinx Programmable Gate Array Registers

The EDT software driver on the host computer uses the following registers (implemented in the Xilinx field-programmable gate array) to control the camera.

NOTE If you're not writing your own driver for the PCI DV, you need not concern yourself with these implementation details.

As the camera data passes through the Xilinx, the firmware performs various operations on it, in the following order. Use the registers described below to affect the data pipeline as follows:

1. Apply the region-of-interest counters if region of interest is enabled in the ROI Control register.
2. If the SWAP_FOR_AIA bit is true in the Shift register, the firmware swaps the 16-bit camera data end for end, so that bit 0 becomes bit 15, bit 1 becomes bit 14, and so on. AIA style cameras place the MSB on VD[0], many non-AIA cameras place the LSB on VD[0].
3. Barrel-shift the 16-bit camera data 0 to 15 places, as determined by the four least significant bits of the Shift register.
4. If the INVERT_DATA bit is true in the Data Path register, invert the data.
5. Zero any bits for which the 16-bit Mask registers have a value of 0.
6. Apply the FILTER_00 or FILTER_FF bits of the Configuration register to clip 8-bit data. If the incoming 16 bits of data represents two 8-bit pixels, both pixels are clipped simultaneously. This clipping operation frees up a few colormap entries for use by the window manager on the host computer, useful when only 256 colormap entries are available on the video display being used.
7. If the EXT_DEPTH bit of the Data Path register is 0, then only bits 0–7 are sent to the host as a single byte; bits 8–15 are ignored.
8. If the BSWAP bit of the Utility register is true, swap every 2 eight bit pixels if EXT_DEPTH is 0, swap the two bytes in each 16 bit pixel if EXT_DEPTH is 1.

Device Control Registers

Command Register

Size	8-bit
I/O	write-only
Address	0x0000.8080
Comments	Bits written to this register are strobe bits and need not be cleared after setting. When read, this register is the Firmware ID register, described next.

Bit	Name	Description
7	STROBE_PIXEL	For debug, setting this bit strobes one pixel of camera data (perhaps from the video data hi/lo registers) out to the host.
6-4	not used	

Bit	Name	Description
3	CLEAR_CONT	Strobe this bit to clear the CONTINUOUS bit of the Data Path register the next time that the ACQUIRE_IP bit in the Status register is true. If ACQUIRE_IP is true when this bit is strobed, CONTINUOUS is cleared immediately.
2	AQ_CLR	Resets ACQUIRE_INT bit of serial data status register.
1	ENABLE_GRAB	Enable acquisition of the next complete frame. If enabled in the configuration register, the shutter time is started. If the continuous acquisition bit is set in the data path register, then ENABLE_GRAB starts acquisition, which continues until the continuous bit is reset.
0	RESET_INTFC	Setting this bit resets the PCI DV interface board.

Firmware ID Register

Size 8-bit

I/O read-only

Address 0x0000.8080

Comments When written, this register is the Command register, described above.

Bit	Name	Description
5–7	not used	
4	VDIO	When true, video data lines can be used for output as well as input.
0–3	REV	The Xilinx firmware revision level.

Status Register

Size 8-bit

I/O read-only

Address 0x0000.8081

Comments The executable *watchstat* (included with the PCI DV software) reads and displays this register symbolically.

Bit	Name	Description
7	ACQUIRE_IP	When set, the camera interface has detected a valid beginning of frame and is presently acquiring data.
6	GRAB_ARMED	When set, the grab command has been issued, any specified hardware trigger has been detected, and the camera interface is waiting for a valid beginning of a frame.
5	CHAN_ID1	Reflects state of the AIA Channel Identification 1 signal.
4	CHAN_ID0	Reflects state of the AIA Channel Identification 0 signal.

Bit	Name	Description
3	TRIGGER_ARMED	When set, the grab command has been issued, and the board is ready for a hardware trigger. Cleared when ACQUIRE_IP goes true unless the ACQUIRE_MULT bit of the Utility2 register is set.
2	EXPOSURE	When set, the camera shutter is open.
1	FRAME_VALID	When set, the camera shutter has closed and valid data is being transmitted (though the PCI DV is not necessarily acquiring data)..
0	OVERRUN	When set, indicates that data was lost during a frame transfer because the host was not ready to receive at the rate at which the camera was transmitting. Therefore the data has been corrupted.

Configuration Register

Size	8-bit
I/O	write-only
Address	0x0000.8082

Bit	Name	Description
7	INT_ENAQ	Setting this bit enables the acquisition interrupt, which occurs with the rising edge of the status register's ACQUIRE_IP bit. Clear the interrupt with the command register's AQ_CLR bit.
6	EN_DALSA	Setting this bit enables DALSA mode. Maps correct signals and polarities out to MC[0-3] for controlling exposure time with PRIN & external sync on Dalsa area scan cameras..
5	FILTER_00	Setting this bit turns on a filter that linearly maps 8 bit pixel values from 0x00–0x0F up into 0x08-0x0F such that 0x00–0x07 are not used. This saves the lowest eight color palette indexes for use by the window manager.
4	FILTER_FF	Setting this bit turns on a filter that linearly maps 8 bit pixel values from 0xF0–0xFF down into 0xF0-0xF7 such that 0xF8–0xFF are not used. This saves the highest eight color palette indexes for use by the window manager.
3	FIFO_RESET	Set and clear this bit to reset the PCI DV input FIFO.
2	INV_SHUTTER	When set, invert the polarity of the shutter signal. The shutter signal is assigned to a mode control signal in the mode register. When cleared, the mode signal is positive when the shutter is open.
1	TRIG	Obsolete; set to 0. Instead, set the shutter timer to the desired length of the trigger pulse, using the Shutter register and the DECADE bits of the Data Path register.
0	DIS_SHUTTER	Obsolete; set to 0. Disable the EXPOSE signal out to the camera by clearing the four most significant bits of the Mode Control register.

Shutter Register

Size	8-bit
I/O	write-only
Address	0x0000.8083

Bit	Description
7–0	Specifies the exposure time –1 (time that the shutter must remain open) in increments of 1 ms, 10 ms or 100 ms: the time base is selected by the DECADE bits in the data path register. If the time base is 1 ms, write 2 for a 3 ms exposure, 4 for a 3 ms exposure, and so on. If the time base is 10 ms, write 2 for a 30 ms exposure.

Table 6. Xilinx Programmable Gate Array Shutter Register**Shutter Time Left Register**

Size	8-bit
I/O	read-only
Address	0x0000.8083
Comments	When written, this is the Shutter register, described above.

Bit	Description
7–0	Specifies the amount of time left before the current exposure terminates.

Data Path Register

Size	8-bit
I/O	read-write
Address	0x0000.8086

Bit	Name	Description															
7-6	DECADE[1-0]	Selects the time base for the shutter counter <table> <thead> <tr> <th>DECADE1</th> <th>DECADE0</th> <th>Time base</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1 millisecond</td> </tr> <tr> <td>0</td> <td>1</td> <td>10 milliseconds</td> </tr> <tr> <td>1</td> <td>0</td> <td>100 milliseconds</td> </tr> <tr> <td>1</td> <td>1</td> <td>reserved</td> </tr> </tbody> </table>	DECADE1	DECADE0	Time base	0	0	1 millisecond	0	1	10 milliseconds	1	0	100 milliseconds	1	1	reserved
DECADE1	DECADE0	Time base															
0	0	1 millisecond															
0	1	10 milliseconds															
1	0	100 milliseconds															
1	1	reserved															
5	INTERLACED	Set if camera is interlaced. In this case, acquisition waits until the first frame valid when the Field ID signal is true.															

Bit	Name	Description
4	CONTINUOUS	Set if PCI DV is to acquire successive frames of data. ENABLE_GRAB in the command register must be set to start acquisition. After CONTINUOUS has been cleared, acquisition continues until the end of a complete frame. Clear in either of two ways: write 0 to this bit to clear it immediately, or strobe the CLEAR_CONT bit of the Command register to clear this bit after the next DMA transfer completes.
3	INVERT_DATA	Inverts the incoming data.
2-1	not used	
0	EXT_DEPTH	Set to send 16 bits to the host for each pixel clock from the camera. Clear to send only the 8 LSB's..

Mode Control Register

Size	8-bit
I/O	read-write
Address	0x0000.8087

Bit	Name	Description
7-4	EN_SHUTTER[3-0]	Selects which mode code signal is driven by the internal signal EXPOSE from the shutter timer. If all of these bits are 0, no EXPOSE signal is sent to the camera. If one of these bits is asserted when in continuous mode, the shutter time asserts EXPOSE to the camera once per frame. This bit is ignored if bit 4 (ENMCOCTL) is set in the Utility register.
3-0	AIA_MC[3-0]	If the output is not enabled as a shutter with the EN_SHUTTER bits above, sets the state of the mode control outputs.

Video Data Lo Register

Size	8-bit
I/O	read-write
Address	0x0000.8088

Bit	Name	Description
7-0	VD[7-0]	Data written to this register is driven out on the 8 data signal pairs to the camera if the VID_DIRECTION bit of the Utility register is 1. When read, it shows the current state of those 8 lines. Note that VD[0] is the LSB of this register, though the AIA cameras place their MSB on this line. (Not available in all Xilinx configuration files.)

Video Data Hi Register

Size	8-bit
I/O	read-write
Address	0x0000.8089

Bit	Name	Description
7-0	VD[15-8]	Data written to this register is driven out on the 8 data signal pairs to the camera if the VID_DIRECTION bit of the Utility register is 1. When read, it shows the current state of those 8 lines. (Not available in all Xilinx configuration files.)

The following three registers implement an asynchronous UART in the Xilinx for communicating with the camera.

NOTE The transmit and receive data lines to the camera are RS-422 differential, not RS-232 levels. Not all cameras use this serial communications channel.

Serial Data Register

Size	8-bit
I/O	read-write
Address	0x0000.808A

Bit	Name	Description
7-0	SERIAL_DATA[0-7]	Data written to this register is output on the Serial Control Out signal if the TRANSMIT_RDY bit is set. Data read from this register reflects the last character received when the RECEIVE_RDY bit is set. (See the serial data status register below for descriptions of these bits.)

Serial Data Status Register

Size	8-bit
I/O	read-write
Address	0x0000.808B

Bit	Name	Description
7	INTFC_INT	INTFC_INT is set when the following boolean expression is true: ((TRANSMIT_RDY and EN_TX_INT) or (RECEIVE_RDY and EN_RX_INT) or ACQUIRE_INT). This expression is then anded with the EN_GLOB_INT bit of the serial data control register and the result passed on to the PCI Xilinx. If the RMT_EN_INTR and PCI_EN_INTR bits of the PCI interrupt and remote Xilinx configuration register in the PCI Xilinx are set (described in the PCIDV user's guide), then an interrupt is asserted over the PCI bus to the host computer.

6	not used	
5	AQUIRE_INT	Set when an acquisition interrupt is enabled through the INT_ENAQ bit of the configuration register, and a rising edge of the AQUIRE_IP bit in the status register has been detected. Clear this interrupt using the AQ_CLR bit of the command register.
4-2	not used	
1	TRANSMIT_RDY	Set when the transmitter is enabled and the holding register is ready for the next character.
0	RECEIVE_RDY	Set when the receiver is enabled and a character is available for reading.

Serial Data Control Register

Size	8-bit
I/O	read-write
Address	0x0000.808C

Bit	Name	Description															
7-6	BAUD[1-0]	Select serial port baud rate for the serial data: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bit 7</th> <th>Bit 6</th> <th>Baud rate</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>9600</td> </tr> <tr> <td>0</td> <td>1</td> <td>19200</td> </tr> <tr> <td>1</td> <td>0</td> <td>38400</td> </tr> <tr> <td>1</td> <td>1</td> <td>115200</td> </tr> </tbody> </table>	Bit 7	Bit 6	Baud rate	0	0	9600	0	1	19200	1	0	38400	1	1	115200
Bit 7	Bit 6	Baud rate															
0	0	9600															
0	1	19200															
1	0	38400															
1	1	115200															
5	CL_RECEIVE_RDY	Set this bit to clear the RECEIVE_RDY bit in the Serial data Status register.															
4	EN_GLOB_INT	Global interrupt enable—enables all interrupts.															
3	EN_TX_INT	Enables the TRANSMIT_RDY interrupt.															
2	EN_RX_INT	Enables the RECEIVE_RDY interrupt.															
1	EN_TX	Enables the serial data transmitter.															
0	EN_RX	Enables the serial data receiver.															

Utility Register

Size	8-bit
I/O	read-write
Address	0x0000.808F

Bit	Name	Description
7	VID_DIRECTION	When 1, drive data from PCIDV to the camera over the video data signal pairs. Data value determined by contents of the registers video data hi and video data low. (Not available with some Xilinx configuration files.)
6	SKIP_X	When 1, skip every other pixel in X to scale image down by 2

5	not used	
4	ENMCOUTL	A value of 0 enables Mode Control output; a value of 1 disables it, allowing the four signal pairs labeled MC[0–3] to be used for incoming data. In this case, values set in the Mode Control register are ignored.
3	SSWAP	A value of 1 swaps the order of 16-bit shorts in a 32-bit word of data coming in from the camera, to accommodate host computer byte order.
2-1	PAD[1-0]	Append 0 to 3 extra pixels at the end of each raster. Use to achieve an even number of 32 bit words per raster to optimize processing of the camera data by the host. (For the special Cincinnati Electronics Xilinx configuration file, when PAD0 is set, every 161st pixel is discarded, yielding 160 pixels per raster on the IRRIS160ST. PAD1 is ignored.)
0	BSWAP	A value of 1 swaps the order of bytes in a 16-bit word of data coming in from the camera, to accommodate host computer byte order.

Hardware Triggering

Hardware triggering provides a way to send a signal over a wire directly to the PCI DV indicating when to acquire a frame. When requested by the application, the driver sets the appropriate hardware trigger bits (0–2) in the Utility2 register and is not further involved with hardware triggering.

The host initiates data acquisition from the camera by strobing the ENABLE_GRAB bit of the Command register. What happens next depends on how the registers have been set; Table 7, “Hardware Triggering” below refers to bit 4 (CONTINUOUS) in the Data Path register (see page 10) and the hardware trigger bits (0–2) in the Utility2 register (starting on page 15).

CONTINUOUS	HWTRIG_CONT	HWTRIGEN_FLDID	HWTRIGEN_OPTO	Description
0		0	0	Acquire the next single frame from the camera.
0	don't care	0	1	Wait for a trigger signal from the user, then acquire a single frame from the camera.
0		1	0	
1	0	0	0	Acquire all subsequent frames from the camera until CONTINUOUS is cleared.
1	0	0	1	Acquire a single frame from the camera for each trigger signal from the user until the CONTINUOUS bit is cleared.
1	0	1	0	
1	1	0	0	Undefined
1	1	0	1	Wait for a trigger signal from the user, then acquire all subsequent frames from the camera until the CONTINUOUS bit is cleared.
1	1	1	0	
don't care	don't care	1	1	Undefined: specify only one hardware trigger source.

Table 7. Hardware Triggering

To use HWTRIGEN_OPTO (the optical coupler) for the hardware trigger source, call EDT and ask for the optical coupler PCI panel. It uses a standard female DB9 connector. Drive the signal into pins 2 and 3 at 5 V, 10 mA; either polarity is acceptable.

To use HWTRIGEN_FLDID (the field ID pins) for the hardware trigger source, drive an RS-422 differential signal into pins 70 (+) and 71 (-) of the camera connector for the PCI DV (pins 24 (+) and 58 (-) for the PCI DVK).

Utility2 Register

Size 8-bit

I/O read-write

Address 0x0000.8090

Comments The ENABLE_GRAB bit in the Command register arms the interface for a single hardware trigger. If no hardware trigger is enabled, then the Xilinx triggers immediately and grabs the next frame of data from the camera. If OPTO_TRIGGER is enabled, then the Xilinx waits until a trigger is received through the optical isolator instead. If FIELDDID_TRIGGER is true, then the Xilinx waits until a trigger is received from the FIELDDID differential pair. If you are using an interlaced camera, the FIELDDID pair is not available for this use.

Once triggered, the Xilinx ordinarily acquires a single frame; if the CONTINUOUS bit is set in the Data Path register, then a single trigger grabs all subsequent frames from the camera.

Bit	Name	Description
7	SELECT_MC4	Setting SELECT_MC4 causes the differential pair normally assigned to SCNTLO (Serial Control Out) to be used instead as a fifth mode control bit.
6	MC4	A fifth mode control bit, used by some Photonics cameras as the Photonics SELECT line.
5	PULNIX	True for all Pulnix cameras. Allows EXPOSE to camera to be asserted even when the incoming FRAME_VALID line is true; waits till the end of EXPOSE before GRAB_ARMED (bit 6 of the Status register) goes true.
4	DBL_TRIG	Enable double trigger mode on the EXPOSE signal out to the camera. Used for some Pulnix model cameras.
3	not used	
2	AQUIRE_MULT	The ENABLE_GRAB bit in the Command register ordinarily arms the interface for a single hardware trigger. Setting AQUIRE_MULT allows a single write to the ENABLE_GRAB bit of the Command register to enable the acquisition of multiple frames, one frame for each hardware trigger from the optical isolator or FIELDDID differential pair.
1	FIELDDID_TRIGGER	When true, you can use the FIELDDID differential pair to trigger data acquisition from the camera, but only after the START bit of the Command register has been strobed.
0	OPTO_TRIGGER	When true, you can use the optical isolator on the PCIDV to trigger data acquisition from the camera, but only after the START bit of the Command register has been strobed.

Shift Register

Size	8-bit
I/O	read-write
Address	0x0000.8091
Comments	The default state of zero causes all 16 bits of camera data to pass through unchanged.

Bit	Name	Description
7-6	not used	
5	MARK09	When true, forces a one on bits 0 and 9 of the 16-bit data path after the mask has been applied. The driver can use this to determine how the host orders bytes during DMA. See the discussion below.
4	SWAP_FOR_AIA	When true, the incoming 16-bit camera data is swapped end for end (bit 0 becomes bit 15, bit 14 becomes bit 1, etc.).
3-0	SHIFT[3-0]	A shift value of 0-15, determining how many places to barrel-shift incoming data downward. For example, a value of 4 moves bits 4-15 down to bits 0-11 (and bits 0-3 around to bits 15-12 where they may subsequently be masked off), suitable for many 12-bit cameras.

The PCI Bus is little-endian. Big-endian hosts sometimes swap byte order during DMA to accommodate the PCI Bus, and sometimes do not. To determine host byte order:

1. Clear the BSWAP and SSWAP bits of the Utility register.
2. Clear the Mask Lo and Mask Hi registers.
3. Use the STROBE_PIXEL bit of the Command register to strobe any 16-bit word into the DMA pipeline. (It will be masked out by the zeroes in the Mask registers.)
4. Set the MARK09 bit of the Shift register (above)—the values of all other bits are irrelevant.
5. Use the STROBE_PIXEL bit of the Command register to strobe another 16-bit word into the DMA pipeline.
6. Have the host perform a DMA read operation of one 32-bit word from the PCI DV.
7. The correct little-endian byte stream for this word is 0x00 0x00 0x01 0x02 (the bits forced to one by the MARK09 bit, above). Determine your result and, if necessary, adjust the BSWAP and SSWAP bits of the Utility register to compensate as required.

Mask Lo Register

Size	8-bit
I/O	read-write
Address	0x0000.8092

Bit	Name	Description
7-0	MASK[7-0]	Bits that are zero force the corresponding camera data bit to zero.

Mask Hi Register

Size	8-bit
I/O	read-write
Address	0x0000.8093

Bit	Name	Description
7-0	MASK[15-8]	Bits that are zero force the corresponding camera data bit to zero.

Region of Interest

Some PCI DV boards support a *region of interest*, a rectangle you can define to crop an image horizontally and vertically, thus eliminating superfluous pixels. To determine whether your board supports this capability:

1. Write a 0 to the Region of Interest Control register.
2. Read the register back. The value returned specifies whether region of interest is supported:

0x00	region of interest, simulator, Dalsa line scan, and dual channel cameras supported
0x80	region of interest, simulator, Dalsa line scan, and dual channel cameras <i>not</i> supported
0xC4	region of interest, simulator, Dalsa line scan, and dual channel cameras <i>not</i> supported; special Xilinx gate array configuration for Iris 256ST and 160ST camera models
other values	undefined

NOTE If region of interest is not supported, then the only part of the ROI Control register available is the bottom three bits, which set the pixel clock rate. The Window registers are also unimplemented unless ROI is supported.

Region of Interest (ROI) Control Register

Size	8-bit
I/O	read-write
Address	0x0000.8097

Comments Besides enabling or disabling a region of interest, use this register to enable or disable Dalsa line scan mode and simulator mode. These bits are not all independent: in particular, simulator mode requires compatible settings: you can run with simulated data (bit 4 true) using either internal or camera timing (bit 5 true or false), but if bit 5 is true, enabling internal timing, then you must also set bit 4 true to use simulated data; otherwise, you will see random pixel data from the camera, as the data and timing will be unsynchronized.

Simulated data is generated as follows:

Data bits 0–7 receive the eight least significant bits of the horizontal pixel count. Bit 7 is inverted once each frame. The data at the start of each raster begins with a value of –2

(0xFE) and counts up. Data bits 8–15 receive the eight least significant bits of the vertical line count, starting with 0x00, and count up.

Simulated data has the least significant bit in data bit 0; therefore, do not set the SWAP_FOR_AIA bit of the Shift register when using the simulator.

Bit	Name	Description																																				
7	DALSA_LS	A value of 1 (true) indicates Dalsa line scan mode, in which the horizontal window registers are used to determine the timing of the EXTSYNC and PRIN lines out to the Dalsa camera. If region of interest is also enabled (see bit 6), the region of interest affects only the number of lines per frame as determined by the vertical window registers; the number of pixels per raster is always as specified by the Dalsa camera.																																				
6	ROI_EN	A value of 1 (true) enables region of interest mode, allowing you to crop the image to a rectangular region of interest. The camera transfers to the host only those pixels in the region of interest, as specified by the window registers.																																				
5	SIM_SYNC	A value of 1 (true) indicates simulator mode. A simulated image of the size specified by the window registers is generated automatically, as if from a camera. To run in simulator mode, also set the SIM_DAT bit to true, and the ROI and DALSA_LS bits to false (0). The pixel clock for the simulator can be either internal or external, as determined by the PCLKSEL bits 2–0.																																				
4	SIM_DAT	A value of 1 (true) indicates that simulated data comes from the window register counters rather than from the camera. You can use simulated data with or without the SIM_SYNC (simulated timing) and PCLKSEL bits.																																				
3	DUAL_CHAN	Set to 1 to enable a data path suitable for dual-channel cameras. Available only for boards that support region of interest capability.																																				
0–2	PCLKSEL	Determines the speed of the clock for the pixel data path: <table border="1" data-bbox="565 1360 1055 1652"> <thead> <tr> <th>Bit 2</th> <th>Bit 1</th> <th>Bit 0</th> <th>Pixel clock rate</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>from camera</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>double rate from camera</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>undefined</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>undefined</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>20 MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>10 MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>5 MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>undefined</td> </tr> </tbody> </table>	Bit 2	Bit 1	Bit 0	Pixel clock rate	0	0	0	from camera	0	0	1	double rate from camera	0	1	0	undefined	0	1	1	undefined	1	0	0	20 MHz	1	0	1	10 MHz	1	1	0	5 MHz	1	1	1	undefined
Bit 2	Bit 1	Bit 0	Pixel clock rate																																			
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1	1	1	undefined																																			

Window Registers

The window registers are 8-bit write-only registers; each set of two stores a 16-bit integer. Assuming region of interest is enabled, together, the window registers specify the size of the region of interest, as described

below. The examples that follow assume a 1024 x 1024 image with a 10-pixel border on all four sides that you wish to crop; thus, a region of interest that is 1004 x 1004.

If you set the SIM_SYNC bit in the ROI Control register, thus enabling simulator mode, and you then write a value to the window registers, the Horizontal and Vertical Skip registers determine the amount of time spent in horizontal and vertical blanking, respectively, and the Horizontal and Vertical Active registers cause the PCI DV to acquire same number of pixels as would be the case if you'd set the ROI_EN bit, thus enabling region-of-interest mode.

If you've enabled Dalsa line scan mode by setting the DALSA_LS bit, the period of the EXTSYNC pulse generated is determined by sum of the Horizontal Skip and Horizontal Active pixel counts. The amount of time that PRIN is asserted is determined by the value in the Horizontal Skip registers. If region of interest is also enabled, then the vertical counters are used to determine how many rasters to skip and how many rasters to acquire.

For more information about EXTSYNC and PRIN, see the Dalsa documentation.

Horizontal Skip Lo and Horizontal Skip Hi Registers

Size 8-bit
 I/O write-only
 Address 0x08098 and 0x8099
 Comments Load these registers with a 16-bit integer specifying the number of pixels to skip at the start of each line. For example, to skip the first 10 pixels of each line, load these registers with the 16-bit value 0x000A.

Bit	Name	Description
7-0	HSKIP[7-0]	Number of pixels to crop at start of each line.

Bit	Name	Description
7-0	HSKIP[15-8]	Number of pixels to crop at start of each line.

Horizontal Active Lo and Horizontal Active Hi Registers

Size 8-bit
 I/O write-only
 Address 0x0809A and 0x809B
 Comments Load these registers with a 16-bit integer specifying the number of pixels to transfer minus 1, on each line, after the blank pixels have been skipped (as specified in Horizontal Skip registers). For example, to acquire 1004 pixels per line, load these registers with 0x03EB.

Bit	Name	Description
7-0	HACT[7-0]	(Number of pixels to transfer)–1 on each line, after blank pixels are skipped.

Bit	Name	Description
7-0	HACT[15-8]	(Number of pixels to transfer)–1 on each line, after blank pixels are skipped.

Vertical Skip Lo and Vertical Skip Hi Registers

Size 8-bit

I/O write-only

Address 0x0809C and 0x809D

Comments Load these registers with a 16-bit integer specifying the number of lines (rasters) to skip at the start of each frame. For example, to skip the first 10 lines of each frame, load these registers with the 16-bit value 0x000A.

Bit	Name	Description
7-0	VSKIP[7-0]	Number of lines to crop at start of each frame.

Bit	Name	Description
7-0	VSKIP[15-8]	Number of lines to crop at start of each frame.

Vertical Active Lo and Vertical Active Hi Registers

Size 8-bit

I/O write-only

Address 0x0809E and 0x809F

Comments Load these registers with a 16-bit integer specifying the number of lines (rasters) to transfer minus 1, on each line, after the blank lines have been skipped (as specified in Vertical Skip registers). For example, to acquire 1004 lines per frame, load these registers with 0x03EB.

Bit	Name	Description
7-0	VACT[7-0]	(Number of lines to transfer)-1 for each frame, after blank lines are skipped.

Bit	Name	Description
7-0	VACT[15-8]	(Number of lines to transfer)-1 for each frame, after blank lines are skipped.

References

Automated Vision Components — Cameras — AIA Monochrome Digital Interface Specification, document # BSR/AIA A15.08/3-199X, available from:

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