

# The PCI DV Camera Link Firmware Reference

The PCI DV Camera Link firmware is intended for the FPGA that communicates with the camera, on a PCI DV Camera Link digital video frame-grabber board. This FPGA is sometimes referred to as the *user interface* (or *UI*) FPGA.

This document describes the connector pinout and registers defined for the following firmware:

<code>pdvcamlk</code>	base-mode firmware for PCI Bus boards
<code>pedvcamlk</code>	base-mode firmware for 4-lane PCI Express Bus boards
<code>pdvcamlk_pir</code>	medium-mode firmware or PCI Bus boards

## Related Documents

The following related publications may prove useful:

Document	URL
EDT DMA & Digital Video Software Library	<a href="http://www.edt.com/api">www.edt.com/api</a> (HTML)
EDT DMA & Digital Video Software Library	<a href="http://www.edt.com/manuals/misc/api.pdf">www.edt.com/manuals/misc/api.pdf</a> (PDF)
PCI DV Family User's Guide	<a href="http://www.edt.com/manuals/PDV/pcidv.pdf">www.edt.com/manuals/PDV/pcidv.pdf</a>
PCI DV Camera Configuration Guide	<a href="http://www.edt.com/manuals/PDV/camconfig.pdf">www.edt.com/manuals/PDV/camconfig.pdf</a>
PCI DV AIA Hardware Addendum	<a href="http://www.edt.com/manuals/PDV/aiag_add_cl2.pdf">www.edt.com/manuals/PDV/aiag_add_cl2.pdf</a>

The Camera Link Specification is available from: [www.machinevisiononline.org](http://www.machinevisiononline.org)

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## Pinouts

The PCI DV C-Link uses two MDR-26 Camera Link connectors. The primary connector is nearest the PCI Bus connector, and is labeled **connector 1**. The secondary connector is labeled **connector 2**.

The primary connector is used for one base-mode camera. The secondary connector can be used for a second base-mode camera, or for the secondary connector of a medium-or full-mode camera.

[Table 1](#) gives the pin assignments for base-, medium-, and full-mode systems.

**Table 1. MDR-26 Pin Assignments**

Camera end	Frame-grabber end	Camera Link signal base mode (primary connector)	Camera Link signal medium mode (secondary connector)	Camera Link signal full mode (secondary connector)
1	1	inner shield	inner shield	inner shield
14	14	inner shield	inner shield	inner shield
2	25	X0-	Y0-	Y0-
15	12	X0+	Y0+	Y0+
3	24	X1-	Y1-	Y1-
16	11	X1+	Y1+	Y1+
4	23	X2-	Y2-	Y2-
17	10	X2+	Y2+	Y2+
5	22	Xclk-	Yclk-	Yclk-
18	9	Xclk+	Yclk+	Yclk+
6	21	X3-	Y3-	Y3-
19	8	X3+	Y3+	Y3+
7	20	SerTC+	unused	100 ohms
20	7	SerTC-	unused	terminated
8	19	SerTFG-	unused	Z0-
21	6	SerTFG+	unused	Z0+
9	18	CC1-	unused	Z1-
22	5	CC1+	unused	Z1+
10	17	CC2+	unused	Z2-
23	4	CC2-	unused	Z2+
11	16	CC3-	unused	Zclk-
24	3	CC3+	unused	Zclk+
12	15	CC4+	unused	Z3-
25	2	CC4-	unused	Z3+
13	13	inner shield	inner shield	inner shield
26	26	inner shield	inner shield	inner shield

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## About the Remote FPGA Registers

This document is of interest to those who wish to understand how the software library routines and camera configuration directives work, and for those writing their own drivers for the PCI DV C-Link. Ordinarily, however, use the higher-level software library routines (documented in the [EDT DMA & Digital Video Software Library](#)) and camera configuration files (documented in the [PCI DV Camera Configuration Guide](#)) to set up the frame-grabber as necessary.

The EDT software driver on the host computer uses the registers described in this document and implemented in the user interface FPGA to control the camera.

As camera data passes through the FPGA, you can use the registers described below to affect the data pipeline as follows:

If region of interest is enabled — that is, the ROI\_DIS bit of the [Camera Link Control Register](#) is false — then the region-of-interest counters apply.

Following the formats described in the Camera Link Specification (online at: [www.machinevisiononline.org](http://www.machinevisiononline.org)), arrange data from the camera into taps as determined by the contents of the [Camera Link Data Path Register](#).

Unless the EXT\_DEPTH bit of the [Data Path Register](#) is set, each tap is truncated to the eight most significant bits, as if the camera were eight bits per tap. Otherwise, you can set the correct number of taps, and bits per tap, for your camera as follows:

- If the RGB bit is set in the [Camera Link Control Register](#), then this overrides any setting in the [Camera Link Data Path Register](#). Data is assumed to come from an RGB color camera with three taps (one each for red, green, and blue) of eight bits each.
- Otherwise, you can set the number of taps and bits per tap in the [Camera Link Data Path Register](#).

In any case, the image data from all taps is packed into 32-bit data words as described in [Table 5 on page 18](#).

The BSWAP and SSWAP bits of the [Utility Register](#) also affect the ordering of the data.

## Camera Interface Registers

Base-mode cameras that are connected to the primary connector can access the registers described below at the primary addresses given. Medium- and full-mode cameras can also use the primary addresses for register access. Only base-mode cameras connected to the secondary connector need to access the registers at the secondary addresses.

### Command Register

Size	8-bit
I/O	write-only
Address	0x00, primary connector 0x40, secondary connector
Access	PCD_CMD
Comments	Bits written to this register do not retain state after writing; there is no need to clear them after setting them. When read, this register is the <a href="#">Firmware ID Register</a> , described next.

Bit	Name	Description
7–5		not used
4	CLRFVINT	Set to clear the Frame Valid interrupt, found in the <a href="#">Serial Data Status Register</a> .
3	CLEAR_CONT	Set to clear the CONTINUOUS bit in the <a href="#">Data Path Register</a> the next time that the ACQUIRE_IP bit in the Status register is set. If ACQUIRE_IP in the <a href="#">Status Register</a> is already set when this bit is toggled, CONTINUOUS is immediately cleared.
2	AQ_CLR	When set, resets the ACQUIRE_INT bit of the <a href="#">Serial Data Status Register</a> .
1	ENABLE_GRAB	Set to cause the frame-grabber to enter the armed state. When armed, the frame-grabber starts acquiring data with the next rising edge of the frame-valid signal. The frame-grabber exits the armed state when data acquisition starts, unless the CONTINUOUS bit is set in the <a href="#">Data Path Register</a> , in which case the frame-grabber remains armed for subsequent frames.
0	RESET_INTFC	Set to reset the PCI DV camera interface circuit. This clears the ACQUIRE and FVAL interrupts, stops current DMA, if any, and returns the board to an idle state.

### Firmware ID Register

Size	8-bit
I/O	read-only
Address	0x00, primary connector 0x40, secondary connector
Access	PDV_REV

Bit	Name	Description
7–4		not used
3–0	REV	The FPGA configuration file revision level.

## Status Register

Size	8-bit
I/O	read-only
Address	0x01, primary connector 0x41, secondary connector
Access	PDV_STAT
Comment	The executable <code>watchstat</code> , included with PCI DV Camera Link software, reads and displays this register symbolically.

Bit	Name	Description
7	AQUIRE_IP	When set, the camera interface has detected a valid beginning of frame and is acquiring data.
6	GRAB_ARMED	When set, the grab command has been issued, any specified hardware trigger has been detected, and the camera interface is waiting for a valid beginning of frame.
5	WIRE_TRIG	Status of incoming trigger on SERTFG2 signal (serial-to-frame-grabber UART signal of secondary connector). If the signal on the secondary connector is not being used for something else, this enables you to use the UART signal pair on the secondary connector as a trigger.
4	PHOTO_TRIG	Status of incoming trigger on photocoupler.
3	TRIGGER_ARMED	When set, the grab command has been issued and the board is ready for a hardware trigger. This bit is cleared when AQUIRE_IP is set, unless the AQUIRE_MULT bit is also set in the Utility 2 Register.
2	EXPOSURE	When set, the camera expose line is asserted.
1	FRAME_VALID	When set, the camera is transmitting a frame of data. This does not necessarily mean that the frame-grabber is acquiring data, which also depends on whether the frame-grabber was armed at the start of the frame.
0	OVERRUN	When set, indicates that data was lost during a frame transfer because the host was not ready to receive at the rate at which the camera was transmitting. Therefore, the data has become corrupted.

## Configuration Register

Size	8-bit
I/O	write-only
Address	0x02, primary connector, 0x42, secondary connector
Access	PDV_CFG

Bit	Name	Description
7	INT_ENAQ	Set to enable the acquisition interrupt, which occurs at the rising edge of the ACQUIRE_IP bit in the <a href="#">Status Register</a> . Clear the interrupt using the AQ_CLR bit in the <a href="#">Command Register</a> .
6–4		not used
3	FIFO_RESET	Toggle this bit to reset the frame-grabber input FIFO.
2	INV_SHUTTER	Set to invert the polarity of the shutter signal. When clear, the selected CC line to the camera is positive to trigger the shutter.  The shutter signal is assigned to the EN_SHUTTER bits in the <a href="#">Mode Control Register</a> .
1–0		not used; always zero

## Shutter Register

Size	8-bit
I/O	write-only
Address	0x03, primary connector 0x43, secondary connector
Access	PDV_SHUTTER
Comment	Many cameras determine the exposure time by a serial UART command; in such cases, the camera uses only the leading edge of the shutter signal, not the trailing edge.

Bit	Name	Description
7–0	SHUTTER[7–0]	Specifies the exposure time minus one, in increments of 1 millisecond, 10 ms, or 100 ms — the units are specified by the DECADE bits in the <a href="#">Data Path Register</a> .  If units are milliseconds, write a value of 2 for a 3 ms exposure; if units are 10 ms, write a value of 2 for a 30 ms exposure; and so on.

## Shutter Time Left Register

Size	8-bit
I/O	read-only
Address	0x03, primary connector 0x43, secondary connector
Access	PDV_SHUTTER_LEFT

Bit	Name	Description
7–0	SHUTTER_LEFT[7–0]	Reads the amount of time left before the current exposure terminates. The units are specified by the DECADE bits in the <a href="#">Data Path Register</a> .

## Utility 3 Register

Size	8-bit
I/O	read-write
Address	0x05, primary connector 0x45, secondary connector
Access	PDV_UTIL3

Bit	Name	Description
7	FRENA	Use FRATE counter (the <a href="#">Frame Rate Bytes 0, 1, and 2 Registers</a> ) to generate a constant frame rate trigger to the camera. See <a href="#">Table 2</a> .  <b>NOTE</b> To avoid undefined operation, if you set this bit, do not set bit 6 (FVADJ) as well.
6	FVADJ	Use FRATE counter (the <a href="#">Frame Rate Bytes 0, 1, and 2 Registers</a> ) to adjust the length of Frame Valid for holding off next frame. See <a href="#">Table 2</a> .  <b>NOTE</b> To avoid undefined operation, if you set this bit, do not set bit 7 (FRENA) as well.
5–4		not used
3	FVINTPOL	When clear, the Frame Valid interrupt occurs on the falling edge of the frame-valid signal from the camera. When set, the Frame Valid interrupt occurs instead on the rising edge of the signal.
2	EXPINT	Select the EXPOSE signal to camera as the source of the Frame Valid interrupt, instead of the Frame Valid signal from the camera.
1		not used
0	PTRIGINV	When set and then triggered from an external device — either optical or SERTFG2 trigger — the incoming trigger polarity is inverted so that negative is true.

The FRENA and FVADJ bits (bits 6 & 7) interact to define the behavior described in [Table 2](#):

**Table 2. Frame Rate Counter Behavior**

FRENA	FVADJ	Result
0	0	Frame rate counter not used. Ordinarily, camera is triggered only after the end of the frame-valid signal for the previous frame.
0	1	Use the frame rate counter (the <a href="#">Frame Rate Bytes 0, 1, and 2 Registers</a> ) to adjust the duration of the frame-valid signal.  Useful for cameras that need an additional delay after frame-valid goes false before triggering the next frame: in such cases, set the frame rate counter for a time period longer than that of frame-valid from the camera.  For cameras able to accept a new trigegr signal while the previous frame-valid signal is still true, set the counter for a time period shorter than the frame-valid signal.
1	0	Use the frame rate counter to specify a constant frame rate (in microseconds).
1	1	undefined

## Data Path Register

Size	8-bit
I/O	read-write
Address	0x06, primary connector 0x46, secondary connector
Access	PDV_DATA_PATH

Bit	Name	Description															
7–6	DECADE[1–0]	Specifies the units for the shutter counter:  <table border="1"> <thead> <tr> <th>DECADE1</th> <th>DECADE0</th> <th>Units</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1 millisecond</td> </tr> <tr> <td>0</td> <td>1</td> <td>10 milliseconds</td> </tr> <tr> <td>1</td> <td>0</td> <td>100 milliseconds</td> </tr> <tr> <td>1</td> <td>1</td> <td>reserved</td> </tr> </tbody> </table>	DECADE1	DECADE0	Units	0	0	1 millisecond	0	1	10 milliseconds	1	0	100 milliseconds	1	1	reserved
DECADE1	DECADE0	Units															
0	0	1 millisecond															
0	1	10 milliseconds															
1	0	100 milliseconds															
1	1	reserved															
5		not used															
4	CONTINUOUS	Set if the frame-grabber is to acquire successive frames of data. To start acquisition, ENABLE_GRAB in the <a href="#">Command Register</a> must be set. After this bit is cleared, acquisition continues until the end of the current frame.  Clear this bit in either of two ways: write a 0 to clear it immediately, or toggle the CLEAR_CONT bit of the <a href="#">Command Register</a> to clear this bit after the next DMA transfer completes.															
3–1		not used															
0	EXT_DEPTH	Set to send full camera bit depth to the host for each pixel from the camera. Clear to send only the eight most significant bits of each pixel. This bit is set automatically if the <code>extdepth</code> camera configuration directive is greater than eight in the camera configuration file.															

## Mode Control Register

Size	8-bit
I/O	read-write
Address	0x07, primary connector 0x47, secondary connector
Access	PDV_MODE_CNTL

Bit	Name	Description
7–4	EN_SHUTTER[4–1]	<p>Sets which camera control signal is driven by the internal EXPOSE signal from the shutter timer.</p> <p>If all bits are 0, no EXPOSE signal is sent to the camera.</p> <p>If one of these bits is asserted while the frame-grabber is in continuous mode, the shutter timer asserts EXPOSE to the camera to trigger each frame.</p> <p>Ordinarily, just one of these bits is true (for most cameras, the least significant bit). However, the following combinations select nonstandard behavior:</p> <p>1010 Drives CC1 with the trigger signal from the photocoupler.</p> <p>1011 Drives CC2 from the photocoupler; CC1, CC3, CC4 all forced low.</p> <p>110– Drives CC4 with frame-valid from the camera, for those frames sent to the host. (The – notation for the least significant bit signifies “don’t care”.)</p>
3–0	CC[4–1]	Sets the state of the camera control outputs, unless the output is enabled as a shutter using the EN_SHUTTER bits described above.

## Serial Data Register

Size	8-bit
I/O	read-write
Address	0x0A, primary connector 0x4A, secondary connector
Access	PDV_SERIAL_DATA
Comment	This register and the next two together implement an asynchronous UART in the FPGA for communicating with the camera. Serial control lines are eight data bits, one stop bit, no parity.

Bit	Name	Description
7–0	SERIAL_DATA[7–0]	<p>If the TRANSMIT_RDY bit is set in the <a href="#">Serial Data Status Register</a>, this register is ready for you to write data to it. The data is then output on the signal SERTC (the serial line to the camera).</p> <p>When the RECEIVE_RDY bit is set in the <a href="#">Serial Data Status Register</a>, data read from this register reflects the last character received.</p>

## Serial Data Status Register

Size	8-bit
I/O	read-only
Address	0x0B, primary connector 0x4B, secondary connector
Access	PDV_SERIAL_DATA_STAT
Comment	This register, the previous one, and the next, together implement an asynchronous UART in the FPGA for communicating with the camera. Serial control lines are eight data bits, one stop bit, no parity.

Bit	Name	Description
7	INTFC_INT	Set when: (TRANSMIT_RDY & EN_TX_INT) OR (RECEIVE_RDY & EN_RX_INT) OR ACQUIRE_INT OR FVINTSTAT  The expression that set this bit is then ANDed with the EN_GLOB_INT bit of the <a href="#">Serial Data Control Register</a> ; the result is passed to the PCI FPGA.  An interrupt is then asserted over the PCI Bus to the host computer if two additional bits are set: RMT_EN_INTR and PCI_EN_INTR in the PCI Interrupt and Remote Xilinx Configuration register, described in the <a href="#">PCI SS/GS Main Board User's Guide</a> .
6	FVINT	Set when the Frame Valid interrupt is pending (see <a href="#">Table 3</a> for a list of possible sources). Cleared by CLR FVINT in the <a href="#">Command Register</a> .
5	ACQUIRE_INT	Set when an acquisition interrupt is enabled through the INT_ENAQ bit of <a href="#">Configuration Register</a> , and a rising edge of the ACQUIRE_IP bit in the <a href="#">Status Register</a> has been detected.  Cleared by AQ_CLR bit in the <a href="#">Command Register</a> .
4	FVINTSTAT	Set when FVINT (bit 6) and EN FVINT (bit 3 in the <a href="#">Utility 2 Register</a> ) are both true.
3–2		not used
1	TRANSMIT_RDY	Set when the serial data transmitter is enabled and ready for the next character. Clears automatically when character transmission is complete.
0	RECEIVE_RDY	Set when the serial data receiver is enabled and a character is available for reading. Cleared by the CL_RECEIVE_RDY bit (bit 5) in the <a href="#">Serial Data Control Register</a> .

The source of a frame-valid interrupt signal can be any of six listed in [Table 3](#), depending on the interactions among the FVINTPOL bit and the EXPINT bit in the [Utility 3 Register](#), and the PTRIGINT bit in the [Utility 2 Register](#). When the source occurs, FVINT is set in this register (see bit 6, above).

If the frame-valid interrupt is also enabled (the bit ENFVINT is set in the [Utility 2 Register](#)), then FVINTSTAT (bit 4 in this register) is set and INTFC\_INT (bit 7) is also set. The interrupt is then sent under the circumstances described above for INTFC\_INT.

**Table 3. Frame Valid Interrupt Source**

PTRIGINT	EXPINT	FVINTPOL	Frame-valid interrupt on...
0	0	0	...falling edge of frame-valid signal.
0	0	1	...rising edge of frame-valid signal.
0	1	0	...falling edge of expose signal (typically, from the shutter timer).
0	1	1	...rising edge of expose signal (typically, from the shutter timer).
1	–	0	...falling edge of signal from photocoupler.
1	–	1	...rising edge of signal from photocoupler.

The notation – means that the value of the bit does not affect the result.

## Serial Data Control Register

Size	8-bit
I/O	read-write
Address	0x0C, primary connector 0x4C, secondary connector
Access	PDV_SERIAL_DATA_CNTL
Comment	This register and the previous two together implement an asynchronous UART in the FPGA for communicating with the camera. Serial control lines are eight data 0bits, one stop bit, no parity.

Bit	Name	Description															
7–6	BAUD[1–0]	Set the serial port baud rate for serial data: <table border="1" data-bbox="552 1228 950 1386"> <thead> <tr> <th>BAUD1</th> <th>BAUD0</th> <th>Baud Rate</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>9600</td> </tr> <tr> <td>0</td> <td>1</td> <td>19200</td> </tr> <tr> <td>1</td> <td>0</td> <td>38400</td> </tr> <tr> <td>1</td> <td>1</td> <td>115200</td> </tr> </tbody> </table> <p>If these choices are insufficient, you can override this value and set an arbitrary baud rate using the <a href="#">Baud Rate Register</a>.</p>	BAUD1	BAUD0	Baud Rate	0	0	9600	0	1	19200	1	0	38400	1	1	115200
BAUD1	BAUD0	Baud Rate															
0	0	9600															
0	1	19200															
1	0	38400															
1	1	115200															
5	CL_RECEIVE_RDY	Set to clear the RECEIVE_RDY bit in the <a href="#">Serial Data Status Register</a> .															
4	EN_GLOB_INT	Enables all interrupts.															
3	EN_TX_INT	Enables the TRANSMIT_RDY interrupt.															
2	EN_RX_INT	Enables the RECEIVE_RDY interrupt.															
1	EN_TX	Enables the serial data transmitter.															
0	EN_RX	Enables the serial data receiver.															

### Utility Register

Size	8-bit
I/O	read-write
Address	0x0F, primary connector 0x4F, secondary connector
Access	PDV_UTILITY

Bit	Name	Description
7–6		not used
5	HWTRIGEXP	When set, the EXPOSE line to the camera comes from the user’s trigger input, either through the photocoupler or from SERTFG2, depending on the HWTRIG bits in the Utility 2 register.  Which of the four camera control lines carries the EXPOSE signal to the camera is determined by the <a href="#">Mode Control Register</a> EN_SHUTTER bits.
4		not used
3	SSWAP	Swaps the order of the two 16-bit short words in one 32-bit data word, so that <i>short 2</i> is transferred before <i>short 1</i> (equivalent to a byte order of 3,4,1,2). Does not change the order of the bits within each short. See <a href="#">Figure 1</a> .
2–1		not used
0	BSWAP	Swaps the order of bytes 1 and 2, and also bytes 3 and 4, in a 32-bit data word, so that the bytes are transferred in the order 2, 1, 4, 3. Does not change the order of the bits within each byte. See <a href="#">Figure 1</a> .

[Figure 1](#) shows the structure of a 32-bit data word.

**Figure 1. Data Word Structure**

short 1																short 2															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
byte 1								byte 2								byte 3								byte 4							

### Hardware Triggering

By default, each time the application sets the ENABLE\_GRAB bit in the [Command Register](#), the camera interface grabs a single frame from the camera. However, if the CONTINUOUS bit in the [Data Path Register](#) is also set, then the camera interface instead grabs successive frames continuously, as quickly as possible.

Hardware triggering provides additional flexibility. After the ENABLE\_GRAB bit is set, acquisition is delayed until a hardware trigger is received. What happens next depends on how the interface is configured: it can grab a single frame, a single frame for each hardware trigger, or grab frames continuously after a single hardware trigger.

The photocoupler on the EDT frame-grabber is ordinarily the source of the hardware trigger. An easy way to connect to the frame-grabber’s photocoupler pins is to use the PCI (or PCIe) trigger input backpanel, EDT part number 017-02792-00. It uses a standard female DB-9 connector. Drive the signal into pins 2 and 3 of the DB-9 connector at 5 V, 10 mA; either polarity is acceptable.

You can determine the state of the SERTFG2 line by reading the WIRETRIG bit (bit 5) of the [Status Register](#).

To use the SERTFG2 signal as the hardware trigger source, see [Table 4](#). [Table 4](#) presents the different kinds of hardware triggering possible, and the bit combinations necessary to use them. The CONTINUOUS bit is in the [Data Path Register](#); the others are in the [Utility 2 Register](#). Bit combinations not shown are undefined.

**Table 4. Hardware Triggering**

Description	CONTINUOUS	HWTRIG2	HWTRIG1	HWTRIG0
Acquire the next single frame.	0	0	0	0
Wait for a trigger signal from the application, then acquire a single frame.	0	0	0	1
Wait for a trigger signal from the SERTFG2 signal, then acquire a single frame.	0	0	1	0
Acquire frames continuously.	1	0	0	0
Acquire a frame for each photocoupler trigger.	1	0	0	1
Acquire a frame for each SERTFG2 trigger.	1	0	1	0
Wait for a trigger signal from the photocoupler, then acquire frames continuously.	1	1	0	1
Wait for a trigger signal from the SERTFG2 signal, then acquire frames continuously.	1	1	1	0

## Utility 2 Register

Size	8-bit
I/O	read-write
Address	0x10, primary connector 0x50, secondary connector
Access	PDV_UTIL2

Bit	Name	Description
7–6		not used
5	PULNIX	Set for some Pulnix cameras — see our default camera configuration file for your model, or the Pulnix camera documentation. Allows EXPOSE to the camera to be asserted even when the incoming Frame Valid line is true; waits until the end of EXPOSE before GRAB_ARMED (bit 6 of the <a href="#">Status Register</a> ) goes true.
4	PTRIGINT	Set to select the photocoupler as the source of the frame-valid interrupt.
3	ENFVINT	Set to enable the Frame Valid interrupt, which ordinarily occurs on the falling edge of Frame Valid. Clear with CLRFVINT in the <a href="#">Command Register</a> .
2–0	HWTRIG[2–0]	Selects kind of hardware triggering, as shown in <a href="#">Table 4</a> .

## Frame Rate Bytes 0, 1, and 2 Registers

Size	8-bit (24-bit in all)
I/O	read-write
Address	0x14, 0x15, 0x16, primary connector 0x54, 0x55, 0x56, secondary connector
Access	PDV_FRAME_PERIOD0, PDV_FRAME_PERIOD1, PDV_FRAME_PERIOD2

Bit	Name	Description
23–0	FRATE[23–0]	<p>A 24-bit preloaded value for the frame rate counter. The counter counts down using microsecond units. For a constant frame rate of <math>n</math> microseconds, preload these registers with <math>n-2</math>. For example, for a constant frame rate of one hundred frames per second (10,000 <math>\mu</math>sec per frame), preload a value of 9998, or 0x00270E.</p> <p>These bits are also used to adjust the frame-valid signal duration so that the frame-grabber can trigger the camera for the next frame either before or after the previous frame has finished transferring.</p> <p>Bits 6 and 7 of the <a href="#">Utility 3 Register</a> determine how the frame rate counter is used. For details, see <a href="#">Table 2 on page 9</a>.</p>

## Region of Interest

The PCI DV Camera Link allows you to define a rectangular region of interest. You can then crop your image horizontally, vertically, or both, to eliminate superfluous pixels.

Unless disabled by the ROIDIS bit in the [Camera Link Control Register](#), the region of interest logic is available. If you wish to acquire the full image, set the region of interest to the full size. Or, you can set the region of interest to be larger than the frame size, to stretch the line-valid and frame-valid signals past the point at which they would ordinarily end.

The region of interest registers are 16-bit write-only registers. Assuming that region of interest has not been disabled, together, these registers define the size of the region of interest.

The examples below assume an image 1024 pixels wide and high with a 10-pixel border on all four sides that you wish to crop; thus, the region of interest is 1004 by 1004.

### Horizontal Skip Register

Size	16-bit
I/O	write-only
Address	0x18, primary connector 0x58, secondary connector
Access	PDV_HSKIP

Bit	Name	Description
15–0	HSKIP[15–0]	Write a 16-bit integer to specify the number of pixels to skip at the start of each line. For example, to skip the first ten pixels of each line, load with 0x000A.

### Horizontal Active Register

Size	16-bit
I/O	write-only
Address	0x1A, primary connector 0x5A, secondary connector
Access	PDV_HACTV

Bit	Name	Description
15–0	HACT[15–0]	Write a 16-bit integer to specify the number of pixels minus one ( <i>pixels</i> – 1) to transfer on each line, after the HSKIP pixels have been skipped. For example, to acquire 1004 pixels on each line, load with 0x03EB.

### Vertical Skip Register

Size	16-bit
I/O	write-only
Address	0x1C, primary connector 0x5, secondary connector
Access	PDV_VSKIP

Bit	Name	Description
15–0	VSKIP[15–0]	Write a 16-bit integer to specify the number of lines to skip at the start of each frame. For example, to skip the first ten lines of each frame, load with 0x000A.

**Vertical Active Register**

Size	16-bit each
I/O	write-only
Address	0x1E, primary connector 0x5E, secondary connector
Access	PDV_VACTV

Bit	Name	Description
15–0	VACT[15–0]	Write a 16-bit integer to specify the number of lines minus one ( <i>lines</i> – 1) to transfer in each frame, after the VSKIP lines have been skipped. For example, to acquire 1004 lines in each frame, load with 0x03EB.

**Baud Rate Register**

Size	8-bit
I/O	read-write
Address	0x24, primary connector 0x 64, secondary connector
Access	PDV_BRATE

Bit	Name	Description
7–0	BRATE[7–0]	<p>Sets the UART baud rate to the value specified. A value of zero specifies that the UART baud rate is set by BAUD[1–0] in the <a href="#">Serial Data Control Register</a>.</p> <p>Given a required baud rate of <i>baud_rate</i>:</p> $\text{BRATE}[7-0] = (20 \text{ MHz} / (\text{baud\_rate} * 16)) - 2$ <p>Round to the nearest integer; however, ensure that such rounding introduces an error less than 5%. (This is a problem only for high baud rates.) If the error is greater than 5%, the camera serial control may not operate reliably.</p> <p>For example, to set a baud rate of 9600:</p> $20000000 / (9600 * 16) - 2 = 128.2$ <p>so load this register with the value 0x80.</p>

## Camera Link Data Path Register

Size	8-bit
I/O	read-write
Address	0x28, primary conenctor 0x78, secondary connector
Access	PDV_CL_DATA_PATH
Comment	Describes the camera in use (numbers of taps and bits per tap) so that the data path can be set up accordingly. This register is loaded automatically according to the setting of the CL_DATA_PATH_NORM directive in the camera configuration file, if one is present.

Only those values listed in [Table 5](#) are supported; all others give undefined results.

Bit	Name	Description
7		not used
6–4	NUMCHAN[3–0]	The number of data taps, minus one.  Three-tap RGB cameras (8 bits per tap, 24 bits per pixel) must not set this to two, but instead, set the RGB bit in the <a href="#">Camera Link Control Register</a> .
3–0	BITS[3–0]	The number of bits per tap, minus one.  Three-tap RGB cameras (8 bits per tap, 24 bits per pixel) must not set this to seven, but instead, set the RGB bit in the <a href="#">Camera Link Control Register</a> .

**NOTE** If the RGB bit is set in the [Camera Link Control Register](#), the setting of this register is ignored.

For efficient DMA transfer, image data from all taps is packed into 32-bit (PCI Bus) or 64-bit (PCI Express Bus) DMA transfer words as follows:

**Table 5. Data Packing**

Number of taps	Bits per tap	Packing
1	8	one byte per Camera Link clock cycle until enough bytes accumulate to fill DMA transfer word
2	8	two bytes per Camera Link clock cycle until enough bytes accumulate to fill DMA transfer word
1	10, 12, 14, 16	two bytes per Camera Link clock cycle in least significant bits of short (16-bit) DMA transfer words, with zeroes as padding in most significant bits as needed.
2	10, 12, 14, 16	four bytes per Camera Link clock cycle in least significant bits of short (16-bit) data words; see <a href="#">Figure 2</a>
3	8	three bytes per Camera Link clock cycle, densely packed; see <a href="#">Figure 3</a> .  <b>NOTE</b> Requires setting the RGB bit in the <a href="#">Camera Link Control Register</a> instead of using the <a href="#">Camera Link Data Path Register</a> .
4 (medium-mode)	8	four bytes per Camera Link clock cycle, no padding. Happens automatically as a consequence of loading the frame-grabber with medium-mode firmware.

Figure 2 shows the structure of a 32-bit data word for a dual-tap camera with 12 bits per pixel, where x represents data and 0 represents padding:

**Figure 2. Data Word Structure, 2-tap 12-bit Camera**

second tap														first tap																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	x	x	x	x	x	x	x	x	x	x	x	x

Figure 3 shows the structure of three consecutive 32-bit data words for a 3-tap RGB camera with eight bits per pixel:

**Figure 3. Data Word Structure, 3-tap 8-bit (RGB) Camera**

second pixel								first pixel																							
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	R	R	B	B	B	B	B	B	B	B	G	G	G	G	G	G	G	G	R	R	R	R	R	R	R	R

third pixel														second pixel																	
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
G	G	G	G	G	G	G	G	R	R	R	R	R	R	R	R	B	B	B	B	B	B	B	B	G	G	G	G	G	G	G	G

fourth pixel																third pixel															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B	B	B	B	B	B	B	B	G	G	G	G	G	G	G	G	R	R	R	R	R	R	R	R	B	B	B	B	B	B	B	B

## Camera Link Control Register

Size	8-bit
I/O	read-write
Address	0x29, primary connector 0x69, secondary connector
Access	PDV_CL_CFG
Comment	This register is loaded automatically according to the setting of the CL_CFG_NORM directive in the camera configuration file, if one is present.

Bit	Name	Description
7	ENROIPAD	<p>Revision 36 or later of <code>pdvcamlk</code> firmware: Enable region-of-interest padding. As of that revision, if the width or height of incoming data comes up short due to data loss, the region-of-interest logic no longer pads with extra bytes. Set this bit to re-enable the previous functionality.</p> <p>To enable region-of-interest for width only (useful for linescan cameras), set bit 3 (0x08) and bit 7 (0x80).</p> <p><b>NOTE</b> Setting this bit on (or using older firmware) can mask timeouts because lost data is padded before the image reaches the device driver, resulting in a persistent out-of-synch condition. The application will then not be notified when it needs to perform timeout recovery.</p>
6	RGBSWAP	Set to swap red (R) and blue (B) bytes in RGB triplets, so that they become BGR.
5	DVINV	Set to invert the data-valid signal, for the few cameras that require this.
4	FVALGEN	For linescan cameras; enables internal generation of Frame Valid after VACTV lines. Set bit 2 when using this feature.
3	ROIDIS	Set to disable the region of interest counters, thus always acquiring the entire image. (The region of interest counters are set in the <a href="#">Horizontal Skip Register</a> , <a href="#">Horizontal Active Register</a> , <a href="#">Vertical Skip Register</a> , and <a href="#">Vertical Active Register</a> .)
2	LINESCAN	Set to replace the frame-valid signal from the camera with a copy of the line-valid signal instead.
1	IGNDVAL	Set if the camera does not implement the data-valid output signal.
0	RGB	Set if the camera is 24-bit color: 8 bits each per red, green, and blue taps. If this bit is set, it overrides any setting of the <a href="#">Camera Link Data Path Register</a> .

### LED Register

Size	8-bit
I/O	read-write
Address	0x30
Access	PDV_CL_LED
Comment	PCI Express boards ( <code>pedvcamlk</code> ) only. For debugging. The LED is located in the middle of the top edge of the board, and is not visible when the board is inside the host, and the host case is closed.

Bit	Name	Description															
7–3		not used															
2	TOGGLE	If bits 0 and 1 of this register are both set, set this bit to turn LED on, clear this bit to turn LED off.															
1–0	SELECT	Set the state of the LED: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>Bit 0</th> <th>Bit 1</th> <th>LED</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>slow blink</td> </tr> <tr> <td>0</td> <td>1</td> <td>blinks when Frame Valid is high</td> </tr> <tr> <td>1</td> <td>0</td> <td>blinks when Line Valid is high</td> </tr> <tr> <td>1</td> <td>1</td> <td>lit if bit 2 is set, dark when bit 2 is clear</td> </tr> </tbody> </table>	Bit 0	Bit 1	LED	0	0	slow blink	0	1	blinks when Frame Valid is high	1	0	blinks when Line Valid is high	1	1	lit if bit 2 is set, dark when bit 2 is clear
Bit 0	Bit 1	LED															
0	0	slow blink															
0	1	blinks when Frame Valid is high															
1	0	blinks when Line Valid is high															
1	1	lit if bit 2 is set, dark when bit 2 is clear															

### Camera Link Control 2 Register

Size	8-bit
I/O	read-write
Address	0x35, primary connector 0x75, secondary connector
Access	PDV_CL_CFG2
Comment	This register is loaded automatically according to the setting of the <code>CL_CFG2_NORM</code> directive in the camera configuration file, if one is present.

Bit	Name	Description
7–1		not used
0	SEPTRIG	When clear (the default), an input trigger on the TRIG0 pin triggers both outgoing EXPOSE lines, one for each connector (channel).  When set, an input trigger on the TRIG0 pin triggers the EXPOSE line on channel 0, and an input trigger on the TRIG1 pin triggers the EXPOSE line on channel 1.  For details on triggering, see the <a href="#">PCI DV Family User's Guide</a> .