SDV

Remote Camera Interface

Addendum for

AIA Monochrome Digital Camera Interface for Category I, Extended Single-Channel Digital Cameras

008-00904-00

Refer questions or problems with this manual or the hardware or software described herein to:

Engineering Design Team, Inc.
1100 NW Compton Drive, Suite 306
Beaverton, Oregon 97006

Phone (503) 690-1234
FAX (503) 690-1243

Contents

Overview

The SDV Remote Camera Interface (SDV-RCI) is an external module that implements a high-speed interface between an external digital camera and the SBus Configurable DMA Fiber Optic Interface (SCD-FOI) board, by means of a fiber optic cable. The SDV-RCI can contain up to four daughter boards, each of which can communicate with its own camera. The camera interface consists of thirty-six RS-422-compatible driver/receivers per daughter board connected to a Xilinx RAM-based programmable gate array. These driver/receivers can be assigned as inputs or outputs in groups of four. The Xilinx device can be programmed to implement arbitrary interface protocols by executing a program that downloads a bit pattern from a file to the SDV-RCI board.

This document describes the SDV hardware and software specific to the AIA Monochrome Digital Camera with Category I Extended Interface: an AIA-compatible camera with a 68-pin high density connector and RS-422 driver/receivers. It lists the camera-specific files included with the software, provides a connector pinout for the camera end of the cable, and includes information on the registers implemented in the Xilinx gate array.

For complete information on using the SBus Digital Video Board Remote Camera Interface, see the *SDV-RCI User's Guide* (part number 008-00915), for which you can contact Engineering Design Team, Inc. In addition, if you wish further information about the SBus Configurable DMA Fiber Optic Interface (SCD-FOI), see the *SCD-FOI User's Guide* (part number 008-00903).

Included Files

In addition to the files listed in the *SDV-RCI User's Guide* (part number 008-00915), the following file is shipped with the SDV-RCI for the AIA-extended cameras:

`aiaextr.rbt` Firmware for AIA extended single-channel digital cameras.

Connector Pinout

The SDV Remote Camera Interface uses a high-density 80-pin I/O connector. The AIA extended single-channel digital cameras use a 68-pin female high-density connector. The cable provided by EDT adapts the SDV board to the camera.

The 68-pin male cable connector is AMP part number 749621-7, with a shielded backshell (AMP part number 750752-1).

The following pinout diagram describes the connection from the cable to the camera. The connection from the SDV board to the cable is described in the *SDV User's Guide* (part number 008-00411), available from Engineering Design Team, Inc.

AIA Pin	AIA Signal	SDV Signal	AIA Pin	AIA Signal	SDV Signal
1	Ground	Ground	35	Ground	Ground
2	MSB +	MSB0 +	36	MSB –	MSB0 –
3	MSB-1 +	MSB1 +	37	MSB-1 –	MSB1 –
4	MSB-2 +	MSB2 +	38	MSB-2 –	MSB2 –
5	MSB-3 +	MSB3 +	39	MSB-3 –	MSB3 –
6	MSB-4 +	MSB4 +	40	MSB-4 –	MSB4 –
7	MSB-5 +	MSB5 +	41	MSB-5 –	MSB5 –
8	MSB-6 +	MSB6 +	42	MSB-6 –	MSB6 –
9	MSB-7 +	MSB7 +	43	MSB-7 –	MSB7 –
10	MSB-8 +	MSB8 +	44	MSB-8 –	MSB8 –
11	MSB-9 +	MSB9 +	45	MSB-9 –	MSB9 –
12	Ground	Ground	46	Ground	Ground
13	MSB-10 +	MSB10 +	47	MSB-10 –	MSB10 –
14	MSB-11 +	MSB11 +	48	MSB-11 –	MSB11 –
15	MSB-12 +	MSB12 +	49	MSB-12 –	MSB12 –
16	MSB-13 +	MSB13 +	50	MSB-13 –	MSB13 –
17	do not use		51	do not use	
18	do not use		52	do not use	
19	MSB-14 +	MSB14 +	53	MSB-14 –	MSB14 –
20	MSB-15 +	MSB15 +	54	MSB-15 –	MSB15 –
21	reserved		55	reserved	
22	Serial Control Out +	SCNTLO +	56	Serial Control Out –	SCNTLO –
23	Serial Cont. In +	SCNTLI +	57	Serial Cont. In –	SCNTLI –
24	Field ID +	FLDID +	58	Field ID –	FLDID –
25	Frame Enable +	FRME +	59	Frame Enable –	FRME –
26	Line Enable +	LINE +	60	Line Enable –	LINE –
27	Channel ID 0 +	ID0 +	61	Channel ID 0 –	ID0 –
28	Channel ID 1 +	ID1 +	62	Channel ID 1 –	ID1 –
29	Pixel Data Strobe +	PSTRB +	63	Pixel Data Strobe –	PSTRB –
30	Mode Control 0 +	FRMRST / EXP +	64	Mode Control 0 –	FRMRST / EXP –
31	Mode Control 1 +	MC0 +	65	Mode Control 1 –	MC0 –
32	Mode Control 2 +	MC1 +	66	Mode Control 2 –	MC1 –
33	Mode Control 3 +	MC2 +	67	Mode Control 3 –	MC2 –
34	Ground	Ground	68	Ground	Ground

Table 1. Connector Pinout

Xilinx Programmable Gate Array Registers

The Xilinx programmable gate array registers are mapped to SBus addresses 0x0001.00D0 through 0x0001.00DF as accessed through the SCD-FOI board.

Command Register

The Command register is an 8-bit write-only register at address 0x10.

Bit	Name	Description
7–6		not used
5	TRIGGER_EXP	Setting this bit triggers the exposure and enables acquisition.
3-4		not used
2		not used
1	ENABLE_GRAB	The same as TRIGGER_EXP except does not trigger the shutter timer. Use ENABLE_GRAB for cameras with built-in shutter control or continuous output.
0	RESET_INTFC	Setting this bit resets the SDV interface board.

Table 2. Xilinx Programmable Gate Array Command Register

Status Register

The Status register is an 8-bit read-only register at address 0x11. The executable `watchstat` (included with the SDV software) reads and displays this register symbolically.

Bit	Name	Description
7	AQUIRE_IP	When set, the camera is presently acquiring data.
6	GRAB_ARMED	When set, the grab command has been issued and the camera is waiting for a valid beginning of a frame.
5	CHAN_ID1	Reflects state of the AIA Channel Identification 1 signal.
4	CHAN_ID0	Reflects state of the AIA Channel Identification 0 signal.
3	FIELD	Reflects state of the AIA Field ID signal. This signal is undefined for noninterlaced cameras, which do not drive it.
2	EXPOSURE	When set, the camera shutter is open.
1	FRAME_VALID	When set, the camera shutter has closed and valid data is being transmitted.
0	OVERRUN	When set, indicates that data was lost during a frame transfer because the channel was saturated. Therefore the data has been corrupted.

Table 3. Xilinx Programmable Gate Array Status Register

Configuration Register

The Configuration register is an 8-bit read-write register at address 0x12.

Bit	Name	Description
7		not used
6	EN_DATA_OUT	Setting this bit enables the data out register to the RS-422 drivers. Before setting this bit, set the data direction register to enable the drivers and disable the receivers.
5	FILTER_00_ON	Setting this bit turns on a filter that maps all bits from 00–10 such that 00–07 are not used. This saves the lowest eight color palette indexes for use by the window manager. This bit is ignored unless the data path is set to clip the camera resolution to 8 bits.
4	FILTER_F0_ON	Setting this bit turns on a filter that maps all bits from F0–FF such that F8–FF are not used. This saves the highest eight color palette indexes for use by the window manager. This bit is ignored unless the data path is set to clip the camera resolution to 8 bits.
3	FIFO_RESET	Set and clear this bit to reset the input FIFOs implemented in the Xilinx.
2	KDK_MC2	When a Kodak Megaplus Camera is under computer control, this bit controls the MC2 signal. When MC2 is set, the shutter remains open and exposure can be controlled by means of a strobe light. These bits are disabled when the DIS_KDK bit is set in the mode control register.
1	KDK_MC1	When a Kodak Megaplus Camera is under computer control, this bit controls the MC1 signal. When MC1 is set, the shutter is open for the time specified by means of the front panel, and the shutter is triggered continuously. The camera therefore takes and transfers one picture after another. When MC1 is not set, the behavior of the camera depends upon the setting of MC0 (see below).
0	KDK_MC0	When a Kodak Megaplus Camera is under computer control, this bit controls the MC0 signal. When MC0 is set and MC1 is not, exposure is triggered by a signal from the computer, and the shutter is open for the time specified using the front panel. When neither MC0 nor MC1 is set, exposure is triggered by a signal from the computer and the shutter is open for the time specified by the shutter register.

Table 4. Xilinx Programmable Gate Array Configuration Register

Shutter Register

The Shutter register is an 8-bit read-write register at address 0x13.

Bit	Description
7–0	Specifies the exposure time (time that the shutter must remain open) in increments of 1 ms, 10 ms or 100 ms. The time base is selected in the data path register (discussed below).

Table 5. Xilinx Programmable Gate Array Shutter Register

Shutter_Time_Left Register

The Shutter_Time_Left register is an 8-bit read-only register at address 0x14.

Bit	Description
7–0	Specifies the amount of time left before the current exposure terminates.

Table 6. Xilinx Programmable Gate Array Shutter_Time_Left Register

Data_Path Register

The Data_Path register is an 8-bit read-write register at address 0x16.

Bit	Name	Description
7-6	DECADE[1-0]	Selects the time base for the shutter counter DECADE1 DECADE0 Time base 0 0 1 millisecond 0 1 10 milliseconds 1 0 100 milliseconds 1 1 reserved
5	FIELD_ID_POL	Specifies the state of the Field ID signal on the first frame enable of an interlaced camera. This bit is significant only if the INTERLACED bit is set (see below).
4	INTERLACED	Set if camera is interlaced. In this case the acquisition waits until the first frame enable when the Field ID signal is at the state specified above in FIELD_ID_POL.
3	not used	Reserved
2-1	RES[1-0]	Set for maximum depth resolution of the camera—the number of shades of gray it can display. RES1 RES0 Resolution Shades of Gray 0 0 12-bit 4096 0 1 10-bit 1024 1 0 16-bit 65,536 1 1 14-bit 16,384
0	EXT_DEPTH	Set when operating the camera in the maximum depth resolution. Cleared when operating in 8-bit mode. In 8-bit mode the most significant 8 bits of data are extracted from each pixel and packed in bytes. Always clear for 8-bit cameras.

Table 7. Xilinx Programmable Gate Array Data_Path Register

Mode_Control Register

The Mode_Control register is an 8-bit read-write register at address 0x17.

Bit	Name	Description
7-6	MC_SHUTTER[1-0]	Selects which mode code signal is driven by the shutter signal when the EN_SHUTTER bit is set (see below).
5	EN_SHUTTER	When set, enables the shutter timer to drive the mode code signal set by bit 6 and 7.
4	DIS_KDK	When set, disables Kodak interpretation of mode codes and drive mode code signals as described in this register. When clear, AIA mode code signal 0 is set by the shutter timer and codes 1–3 are set by the shutter control signals in configuration register.
3-0	AIA_MC[3-0]	If the DIS_KDK bit is set, sets the state of the AIA mode control outputs. One of these signals can be driven from the shutter timer if EN_SHUTTER is set and the signal is selected with the MC_SHUTTER[1-0].

Table 8. Xilinx Programmable Gate Array Mode_Control Register

Data_Out Register

The Data_Out register is an 16-bit read-write register at address 0x18.

Bit	Name	Description
15-0	DATA_OUT[15-0]	If data output is selected and the Data Direction register is set properly, data output on the external data lines. (See the *SDV User's Guide* for the proper settings.)

Table 9. Xilinx Programmable Gate Array Data_Out Register

Serial_Data Register

The Serial_Data register is an 8-bit read-write register at address 0x1A.

Bit	Name	Description
7-0	SERIAL_DATA[7-0]	Data written to this register is output on the AIA Serial Control Out signal if the TRANSMIT_RDY bit is set. Data read from this register reflects the last character received when the RECEIVE_RDY bit is set. (See the serial data status register below for descriptions of these bits.)

Table 10. Xilinx Programmable Gate Array Serial_Data Register

Serial_Enable Register

The Serial_Enable register is an 8-bit write-only register at address 0x1B.

Bit	Name	Description
0	RECEIVE_EN	Enable the serial data receiver
1	TRANSMIT_EN	Enable the serial data transmitter.
2–7		not used

Table 11. Xilinx Programmable Gate Array Serial_Enable Register

Interrupts

When a condition occurs that requires a host interrupt, a write automatically occurs over the fiber optic cable to the SCD-FOI's remote flag register. The interrupt control registers on the SCD-FOI then determine if an interrupt is asserted out to the SBus.

As soon as the SDV-RCI writes to the SCD-FOI remote flag register, no additional remote flag writes will occur until the interrupt is serviced by a write to the remote camera interface's Interrupt_Enable register described below. The ACQUIRE bit id usually used to tell the host that the camera has acquired the current image and is starting to send it, giving the host permission to send the command to open the camera's shutter for the next image.

Interrupt_Source Register

The Interrupt_Source register is an 8-bit read-only register at address 0x1C, used to implement interrupts on behalf of the remote device. Write all ones to clear this register to all zeroes.

Bit	Name	Description
D0	RECEIVE_RDY	True when the serial data receive buffer is full.
D1	TRANSMIT_RDY	True when the serial data transmit buffer is empty.
D2	ACQUIRE	True when the camera starts to send image data.
D3–7		not used

Table 12. Xilinx Programmable Gate Array Interrupt_Source Register

Interrupt_Enable Register

The Interrupt_Enable register is an 8-bit read-write register at address 0x1D. Reading this register returns the last data written.

Bit	Name	Description
D0	RECEIVE_RDY	Enable interrupts on the RECEIVE_RDY bit in the Interrupt_Source register.
D1	TRANSMIT_RDY	Enable interrupts on the TRANSMIT_RDY bit in the Interrupt_Source register.
D2	ACQUIRE	Enable interrupts on the ACQUIRE bit in the Interrupt_Source register.
D3–7		not used

Table 13. Xilinx Programmable Gate Array Interrupt_Enable Register

Interrupt_Status Register

The Interrupt_Status register is an 8-bit read-only register at address 0x1E. Reading this register returns the result of ANDing the Interrupt Enable and Interrupt Source bits, indicating which bit is initiating an SBus interrupt. The Xilinx firmware automatically writes the contents of this register to the SCD-FOI FOI_Flag register whenever a condition occurs that requires an interrupt.

Bit	Name	Description
D0	RECEIVE_RDY	The result of ANDing the corresponding bits from the Interrupt_Enable and Interrupt_Source registers.
D1	TRANSMIT_RDY	The result of ANDing the corresponding bits from the Interrupt_Enable and Interrupt_Source registers.
D2	ACQUIRE	The result of ANDing the corresponding bits from the Interrupt_Enable and Interrupt_Source registers.
D3–7		not used

Table 14. Xilinx Programmable Gate Array Interrupt_Status Register