

# EDT Pinouts

## Quick Reference

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## Control Information

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## Revision History

Revision	Date	Revision Description	Originator
Draft	05-Sep-02	New document	S Vasil
A	19-Feb-03	Added RCX pinout	D Boer
B	20-Aug-03	Added SSD4IO 68-pin to four DB9 cable pinout	M Mason
C	18-Mar-04	Added CDa pinout	D Boer
D	21-Apr-04	Updated CDa pinout	D Boer
E	12-Jul-04	Fixed GP SSE pinout	J Gaffke
F	9-Sep-04	Fixed CDa pinout	D Boer

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# Overview

This document is intended as a quick reference guide for EDT connector pinout information, and it does not explain each pin function. For additional information on a specific board, see the associated user's guide at [www.edt.com](http://www.edt.com) > Technical > Documentation.

## PCI DV Boards

EDT Board	Board Type	Bitfile	Table Number	Page Number
PCI DV AIA	AIA	aiag.bit	1-3	6
PCI DVK AIA	AIA	aiag.bit	4-6	9
PCI DV44	AIA	aiag.bit	7	12
PCI DV C-LINK	Camera Link	pdvcamlk.bit	8	13
PCI RCI	AIA	aiag_3v.bit aiag_5v.bit	9-11	14
RCX Module	Camera Extender		12	17

## PCI CD Boards

EDT Board	Board Type	Bitfile	Table Number	Page Number	
PCI CD	8-bit parallel	pcd8_src.bit	13	18	
	16-bit parallel	pcd_src.bit	14	19	
		pcd_looped.bit	14		
	1-channel		ssd.bit	15	20 21
			ssdout1.bit	16	
			ssdio.bit	16	
			ssdio_neg.bit	16	
2-channel	ssd2.bit	15	20		
4-channel	ssd4.bit	15	20		
PCI CDa	16-channel	ssd16io.bit	17	22	
PCI GP	8-bit parallel	gp_pcd8.bit	18	23	
	16-bit parallel	gp_pcd.bit	19	24	
	4-channel	gpssd4.bit	20	25	
		ssd4io.bit	21	26	
16-channel	ssd16.bit	22	27		
PCI GP SSE	2-channel	pcdssd.bit	23	28	
PCI SS	16-bit parallel	ss_pcd.bit	19	24	
	16-channel	ssd16in.bit	22	27	
		eclssd.bit	22		
		eclssd16in.bit	22		
16-channel E1/T1	combo16in.bit	24	29		

## EDT Pinouts

EDT Board	Board Type	Bitfile	Table Number	Page Number
	4-channel E3/T3	combo16in.bit	25	30

## Other PCI Boards

EDT Board	Board Type	Bitfile	Table Number	Page Number
PCI 11W	16-bit parallel	p11w_3v.bit p11w_5v.bit	26	31
PCI 16D	16-bit parallel	p16d_3v.bit p16d_5v.bit	27	32
PCI 53B	Avionics Serial (with redundant serial)	xc21b.blk	28	33

# EDT Pinouts

PCI DV Pin	PCI DV Signal	AIA Signal	PCI DV Pin	PCI DV Signal	AIA Signal
1	Ground	Not used	41	Ground	Not used
2	Ground	Not used	42	Ground	Not used
3	VD4 +	MSB4 +	43	VD0 +	MSB0 +
4	VD4 -	MSB4 -	44	VD0 -	MSB0 -
5	VD5 +	MSB5 +	45	VD1 +	MSB1 +
6	VD5 -	MSB5 -	46	VD1 -	MSB1 -
7	VD6 +	MSB6 +	47	VD2 +	MSB2 +
8	VD6 -	MSB6 -	48	VD2 -	MSB2 -
9	VD7 +	MSB7 +	49	VD3 +	MSB3 +
10	VD7 -	MSB7 -	50	VD3 -	MSB3 -
11	VD12 +	MSB12 +	51	VD8 +	MSB8 +
12	VD12 -	MSB12 -	52	VD8 -	MSB8 -
13	VD13 +	MSB13 +	53	VD9 +	MSB9 +
14	VD13 -	MSB13 -	54	VD9 -	MSB9 -
15	VD14 +	MSB14 +	55	VD10 +	MSB10 +
16	VD14 -	MSB14 -	56	VD10 -	MSB10 -
17	VD15 +	MSB15 +	57	VD11 +	MSB11 +
18	VD15 -	MSB15 -	58	VD11 -	MSB11 -
19	Spare16 +	Not used	59	Spare16 -	Not used
20	+5V	Not used	60	+5V	Not used
21	Spare17 +	Not used	61	Spare17 -	Not used
22	Spare18 +	Not used	62	Spare18 -	Not used
23	Ground	Not used	63	Ground	Not used
24	SCNTLO +	Serial Control Out +	64	PSTRB +	Pixel Strobe +
25	SCNTLO -	Serial Control Out -	65	PSTRB -	Pixel Strobe -
26	ID0 +	Channel ID 0 +	66	LINE +	Line Enable +
27	ID0 -	Channel ID 0 -	67	LINE -	Line Enable -
28	ID1 +	Channel ID 1 +	68	FRME +	Frame Enable +
29	ID1 -	Channel ID 1 -	69	FRME -	Frame Enable -
30	Spare7 +	Not used	70	FLDID +	Field ID +
31	Spare7 -	Not used	71	FLDID -	Field ID -
32	SCNTLI +	Serial Control In +	72	MC0 +	Mode Control 0 +
33	SCNTLI -	Serial Control In -	73	MC0 -	Mode Control 0 -
34	Spare13 +	Not used	74	MC1+	Mode Control 1 +
35	Spare13 -	Not used	75	MC1 -	Mode Control 1 -
36	Spare14 +	Not used	76	MC2 +	Mode Control 2 +
37	Spare14 -	Not used	77	MC2 -	Mode Control 2 -
38	EXPOSEB +	Not used	78	EXPOSE +	FRMRST/EXP +
39	EXPOSEB -	Not used	79	EXPOSE -	FRMRST/EXP -
40	Ground	Ground	80	Ground	Ground

**Table 1. PCI DV for Single-channel Grayscale Cameras (aiag.bit)**

*Shading denotes out to camera*



PCI DV Pin	PCI DV Signal	AIA Signal	PCI DV Pin	PCI DV Signal	AIA Signal
1	Ground	Not used	41	Ground	Ground
2	Ground	Not used	42	Ground	Not used
3	VDA4 +	AMSB4 +	43	VDA0 +	AMSB +
4	VDA4 -	AMSB4 -	44	VDA0 -	AMSB -
5	VDA5 +	AMSB5 +	45	VDA1 +	AMSB1 +
6	VDA5 -	AMSB5 -	46	VDA1 -	AMSB1 -
7	VDA6 +	AMSB6 +	47	VDA2 +	AMSB2 +
8	VDA6 -	AMSB6 -	48	VDA2 -	AMSB2 -
9	VDA7 +	AMSB7 +	49	VDA3 +	AMSB3 +
10	VDA7 -	AMSB7 -	50	VDA3 -	AMSB3 -
11	VDB4 +	BMSB4 +	51	VDB0 +	BMSB +
12	VDB4 -	BMSB4 -	52	VDB0 -	BMSB -
13	VDB5 +	BMSB5 +	53	VDB1 +	BMSB1 +
14	VDB5 -	BMSB5 -	54	VDB1 -	BMSB1 -
15	VDB6 +	BMSB6 +	55	VDB2 +	BMSB2 +
16	VDB6 -	BMSB6 -	56	VDB2 -	BMSB2 -
17	VDB7 +	BMSB7 +	57	VDB3 +	BMSB3 +
18	VDB7 -	BMSB7 -	58	VDB3 -	BMSB3 -
19	VDA8 +	AMSB8 +	59	VDB8 -	AMSB8 -
20	+5V	+5V	60	+5V	+5V
21	VDA10 +	AMSB10 +	61	VDA10 -	AMSB10 -
22	VDA11 +	AMSB11 +	62	VDA11 -	AMSB11 -
23	Ground	Ground	63	Ground	Ground
24	SCNTLO +	Serial Control Out +	64	PSTRB +	Pixel Strobe +
25	SCNTLO -	Serial Control Out -	65	PSTRB -	Pixel Strobe -
26	VDB10 +	BSMB10 +	66	LINE +	Line Enable +
27	VDB10 -	BSMB10 -	67	LINE -	Line Enable -
28	ID1 +	Bloomflag +	68	FRME +	Frame Enable +
29	ID1 -	Bloomflag -	69	FRME -	Frame Enable -
30	Spare7 +	TRIG +	70	VDB11 +	BMSB11 +
31	Spare7 -	TRIG -	71	VDB11 -	BMSB11 -
32	SCNTLI +	Serial Control In +	72	VDA9 +	AMSB9 +
33	SCNTLI -	Serial Control In -	73	VDA9 -	AMSB9 -
34	Spare13 +	Not used	74	VDB8 +	BMSB8 +
35	Spare13 -	Not used	75	VDB8 -	BMSB8 -
36	Spare14 +	Not used	76	VDB9 +	BMSB9 +
37	Spare14 -	Not used	77	VDB9 -	BMSB9 -
38	EXPOSEB +	FRMRST/EXP +	78	EXPOSE +	Not used
39	EXPOSEB -	FRMRST/EXP -	79	EXPOSE -	Not used
40	Ground	Ground	80	Ground	Ground

**Table 2. PCI DV for Dual-channel Grayscale Cameras (aiag.bit)**

*Shading denotes out to camera.*



## EDT Pinouts

PCI DV Pin	PCI DV Signal	AIA Signal	PCI DV Pin	PCI DV Signal	AIA Signal
1	Ground	Not used	41	Ground	Not used
2	Ground	Not used	42	Ground	Not used
3	VDA4 +	RedMSB4 +	43	VDA0 +	RedMSB0 +
4	VDA4 -	RedMSB4 -	44	VDA0 -	RedMSB0 -
5	VDA5 +	RedMSB5 +	45	VDA1 +	RedMSB1 +
6	VDA5 -	RedMSB5 -	46	VDA1 -	RedMSB1 -
7	VDA6 +	RedMSB6 +	47	VDA2 +	RedMSB2 +
8	VDA6 -	RedMSB6 -	48	VDA2 -	RedMSB2 -
9	VDA7 +	RedMSB7 +	49	VDA3 +	RedMSB3 +
10	VDA7 -	RedMSB7 -	50	VDA3 -	RedMSB3 -
11	VDB4 +	GrnMSB4 +	51	VDB0 +	GrnMSB0 +
12	VDB4 -	GrnMSB4 -	52	VDB0 -	GrnMSB0 -
13	VDB5 +	GrnMSB5 +	53	VDB1 +	GrnMSB1 +
14	VDB5 -	GrnMSB5 -	54	VDB1 -	GrnMSB1 -
15	VDB6 +	GrnMSB6 +	55	VDB2 +	GrnMSB2 +
16	VDB6 -	GrnMSB6 -	56	VDB2 -	GrnMSB2 -
17	VDB7 +	GrnMSB7 +	57	VDB3 +	GrnMSB3 +
18	VDB7 -	GrnMSB7 -	58	VDB3 -	GrnMSB3 -
19	VDA8 +	BluMSB0 +	59	VDB8 -	BluMSB0 -
20	+5V	Not used	60	+5V	Not used
21	VDA10 +	AMSB10 +	61	VDA10 -	AMSB10 -
22	VDA11 +	BluMSB4 +	62	VDA11 -	BluMSB4 -
23	Ground	Not used	63	Ground	Not used
24	SCNTLO +	Serial Control Out +	64	PSTRB +	Pixel Strobe +
25	SCNTLO -	Serial Control Out -	65	PSTRB -	Pixel Strobe -
26	VDB10 +	BluMSB6 +	66	LINE +	Line Enable +
27	VDB10 -	BluMSB6 -	67	LINE -	Line Enable -
28	ID1 +	BluMSB7 +	68	FRME +	Frame Enable +
29	ID1 -	BluMSB7 -	69	FRME -	Frame Enable -
30	Spare7 +	Not used	70	VDB11 +	BluMSB5 +
31	Spare7 -	Not used	71	VDB11 -	BluMSB5 -
32	SCNTLI +	Serial Control In +	72	VDA9 +	BluMSB1 +
33	SCNTLI -	Serial Control In -	73	VDA9 -	BluMSB1 -
34	Spare13 +	Not used	74	VDB8 +	BluMSB2 +
35	Spare13 -	Not used	75	VDB8 -	BluMSB2 -
36	Spare14 +	Not used	76	VDB9 +	BluMSB3 +
37	Spare14 -	Not used	77	VDB9 -	BluMSB3 -
38	EXPOSEB +	FRMRST/EXP +	78	EXPOSE +	Not used
39	EXPOSEB -	FRMRST/EXP -	79	EXPOSE -	Not used
40	Ground	Ground	80	Ground	Ground

**Table 3. PCI DV for Single-channel Color Cameras (aiag.bit)**

*Shading denotes out to camera.*

## EDT Pinouts

PCI DVK Pin	PCI DVK Signal	AIA Signal	PCI DVK Pin	PCI DVK Signal	AIA Signal
1	Spare	Spare	35	Spare	Spare
2	VD0 +	MSB +	36	VD0 –	MSB –
3	VD1 +	MSB1 +	37	VD1 –	MSB1 –
4	VD2 +	MSB2 +	38	VD2 –	MSB2 –
5	VD3 +	MSB3 +	39	VD3 –	MSB3 –
6	VD4 +	MSB4 +	40	VD4 –	MSB4 –
7	VD5 +	MSB5 +	41	VD5 –	MSB5 –
8	VD6 +	MSB6 +	42	VD6 –	MSB6 –
9	VD7 +	MSB7 +	43	VD7 –	MSB7 –
10	VD8 +	MSB8 +	44	VD8 –	MSB8 –
11	VD9 +	MSB9 +	45	VD9 –	MSB9 –
12	Spare	Spare	46	Spare	Spare
13	VD10 +	MSB10 +	47	VD10 –	MSB10 –
14	VD11 +	MSB11 +	48	VD11 –	MSB11 –
15	VD12 +	MSB12 +	49	VD12 –	MSB12 –
16	VD13 +	MSB13 +	50	VD13 –	MSB13 –
17	Spare17 +	Not used	51	Spare17 –	Not used
18	Spare18 +	Not used	52	Spare18 –	Not used
19	VD14 +	MSB14 +	53	VD14 –	MSB14 –
20	VD15 +	MSB15 +	54	VD15 –	MSB15 –
21	Spare16 +	Reserved	55	Spare16 –	Reserved
22	SCNTLO +	Serial Control Out +	56	SCNTLO –	Serial Control Out –
23	SCNTLI +	Serial Control In +	57	SCNTLI –	Serial Control In –
24	FLDID +	Field ID +	58	FLDID –	Field ID –
25	FRME +	Frame Enable +	59	FRME –	Frame Enable –
26	LINE +	Line Enable +	60	LINE –	Line Enable –
27	ID0 +	Channel ID 0 +	61	ID0 –	Channel ID 0 –
28	ID1 +	Channel ID 1 +	62	ID1 –	Channel ID 1 –
29	PSTRB +	Pixel Strobe +	63	PSTRB –	Pixel Strobe –
30	EXPOSE +	Mode Control 0 +	64	EXPOSE –	Mode Control 0 –
31	MC0 +	Mode Control 1 +	65	MC0 –	Mode Control 1 –
32	MC1 +	Mode Control 2 +	66	MC1 –	Mode Control 2 –
33	MC2 +	Mode Control 3 +	67	MC2 –	Mode Control 3 –
34	Ground	Ground	68	Ground	Ground

**Table 4. PCI DVK for Single-channel Grayscale Cameras (aiag.bit)**

*Shading denotes out to camera.*

## EDT Pinouts

PCI DVK Pin	PCI DVK Signal	AIA Signal	PCI DVK Pin	PCI DVK Signal	AIA Signal
1	Spare	Spare	35	Spare	Spare
2	VDA0 +	AMSB +	36	VDA0 –	AMSB –
3	VDA1 +	AMSB1 +	37	VDA1 –	AMSB1 –
4	VDA2 +	AMSB2 +	38	VDA2 –	AMSB2 –
5	VDA3 +	AMSB3 +	39	VDA3 –	AMSB3 –
6	VDA4 +	AMSB4 +	40	VDA4 –	AMSB4 –
7	VDA5 +	AMSB5 +	41	VDA5 –	AMSB5 –
8	VDA6 +	AMSB6 +	42	VDA6 –	AMSB6 –
9	VDA7 +	AMSB7 +	43	VDA7 –	AMSB7 –
10	VDB0 +	BMSB +	44	VDB0 –	BMSB –
11	VDB1 +	BMSB1 +	45	VDB1 –	BMSB1 –
12	Spare	Spare	46	Spare	Spare
13	VDB2 +	BMSB2 +	47	VDB2 –	BMSB2 –
14	VDB3 +	BMSB3 +	48	VDB3 –	BMSB3 –
15	VDB4 +	BMSB4 +	49	VDB4 –	BMSB4 –
16	VDB5 +	BMSB5 +	50	VDB5 –	BMSB5 –
17	Spare17 +	Not used	51	Spare17 –	Not used
18	Spare18 +	Not used	52	Spare18 –	Not used
19	VDB6 +	BMSB6 +	53	VDB6 –	BMSB6 –
20	VDB7 +	BMSB7 +	54	VDB7 –	BMSB7 –
21	VDA8 +	AMSB8 +	55	VDA8 –	AMSB8 –
22	SCNTLO +	Serial Control Out +	56	SCNTLO –	Serial Control Out –
23	SCNTLI +	Serial Control In +	57	SCNTLI –	Serial Control In –
24	FLDID +	Field ID +	58	FLDID –	Field ID –
25	FRME +	Frame Enable +	59	FRME –	Frame Enable –
26	LINE +	Line Enable +	60	LINE –	Line Enable –
27	ID0 +	Channel ID 0 +	61	ID0 –	Channel ID 0 –
28	ID1 +	Channel ID 1 +	62	ID1 –	Channel ID 1 –
29	PSTRB +	Pixel Strobe +	63	PSTRB –	Pixel Strobe –
30	EXPOSE +	EXPOSE 0 +	64	EXPOSE –	EXPOSE –
31	VDA9 +	AMSB9 +	65	VDA9 –	AMSB9 –
32	VDB8 +	BMSB8 +	66	VDB8 –	BMSB8 –
33	VDB9 +	BMSB9 +	67	VDB9 –	BMSB9 –
34	Ground	Ground	68	Ground	Ground

**Table 5. PCI DVK for Dual-channel Grayscale Cameras (aiag.bit)**

*Shading denotes out to camera.*

## EDT Pinouts

PCI DVK Pin	PCI DVK Signal	AIA Signal	PCI DVK Pin	PCI DVK Signal	AIA Signal
1	Spare	Spare	35	Spare	Spare
2	VDR0 +	RedMSB0 +	36	VDR0 –	RedMSB0 –
3	VDR1 +	Red MSB1 +	37	VDR1 –	RedMSB1 –
4	VDR2 +	Red MSB2 +	38	VDR2 –	Red MSB2 –
5	VDR3 +	Red MSB3 +	39	VDR3 –	Red MSB3 –
6	VDR4 +	Red MSB4 +	40	VDR4 –	Red MSB4 –
7	VDR5 +	Red MSB5 +	41	VDR5 –	Red MSB5 –
8	VDR6 +	Red MSB6 +	42	VDR6 –	Red MSB6 –
9	VDR7 +	Red MSB7 +	43	VDR7 –	Red MSB7 –
10	VDG0 +	GrnMSB0 +	44	VDG0 –	GrnMSB0 –
11	VDG1 +	GrnMSB1 +	45	VDG1 –	GrnMSB1 –
12	Spare	Spare	46	Spare	Spare
13	VDG2 +	GrnMSB2 +	47	VDG2 –	GrnMSB2 –
14	VDG3 +	GrnMSB3 +	48	VDG3 –	GrnMSB3 –
15	VDG4 +	GrnMSB4 +	49	VDG4 –	GrnMSB4 –
16	VDG5 +	GrnMSB5 +	50	VDG5 –	GrnMSB5 –
17		not used	51		not used
18	VDB4 +	BluMSB4 +	52	VDB4 –	BluMSB4 –
19	VDB6 +	GrnMSB6 +	53	VDB6 –	GrnMSB6 –
20	VDB7 +	GrnMSB7 +	54	VDB7 –	GrnMSB7 –
21	VDB0 +	BluMSB0 +	55	VDB0 –	BluMSB0 –
22	SCNTLO +	Serial Control Out +	56	SCNTLO –	Serial Control Out –
23	SCNTLI +	Serial Control In +	57	SCNTLI –	Serial Control In –
24	VDB5 +	BluMSB5 +	58	VDB5 –	BluMSB5 –
25	FRME +	Frame Enable +	59	FRME –	Frame Enable –
26	LINE +	Line Enable +	60	LINE –	Line Enable –
27	VDB6 +	BluMSB6 +	61	VDB6 –	BluMSB6 –
28	VDB7 +	BluMSB7 +	62	VDB7 –	BluMSB7 –
29	PSTRB +	Pixel Strobe +	63	PSTRB –	Pixel Strobe –
30	EXPOSE +	EXPOSE +	64	EXPOSE –	EXPOSE –
31	VDB1 +	BluMSB1 +	65	VDB1 –	BluMSB1 –
32	VDB2 +	BluMSB2 +	66	VDB2 –	BluMSB2 –
33	VDB3 +	BluMSB3 +	67	VDB3 –	BluMSB3 –
34	Ground	Ground	68	Ground	Ground

**Table 6. PCI DVK for Single-channel Color Cameras (aiag.bit)**

*Shading denotes out to camera.*

DVC Pin	DVC Name	PCI DV 44 Name
*1	PIXCLK +	PSTRB –
2	Ground	Ground
3	ENF +	FRME +
4	MSB +	VD0 +
5	MSB1 +	VD1 +
6	MSB2 +	VD2 +
7	MSB3 +	VD3 +
8	MSB4 +	VD4 +
9	MSB5 +	VD5 +
10	MSB6 +	VD6 +
11	MSB7 +	VD7 +
12	MSB8 +	VD8 +
13	MSB9 +	VD9 +
14	MSB10 +	VD10 +
15	MSB11 +	VD11 +

DVC Pin	DVC Name	PCI DV 44 Name
*16	PIXCLK –	PSTRB +
17	Ground	Ground
18	ENF –	FRME –
19	MSB –	VD0 –
20	MSB1 –	VD1 –
21	MSB2 –	VD2 –
22	MSB3 –	VD3 –
23	MSB4 –	VD4 –
24	MSB5 –	VD5 –
25	MSB6 –	VD6 –
26	MSB7 –	VD7 –
27	MSB8 –	VD8 –
28	MSB9 –	VD9 –
29	MSB10 –	VD10 –
30	MSB11 –	VD11 –

DVC Pin	DVC Name	PCI DV 44 Name
31	ENL +	LINE +
32	ENL –	LINE –
33	Not used	
34	INPUT1 +	EXPOSE +
35	INPUT1 –	EXPOSE –
**36	R1 IN	SCNTLI
**37	T1 OUT	SCNTLO
38	COM GND	Ground
39	VRST_INT	Not used
40	Reserved	MC2 +
41	Ground	Ground
42	Reserved	MC2 –
43	Ground	Ground
44	Reserved	Not used

**Table 7. PCI DV44 for DVC1310 and DVC1312 Cameras (aiag.bit)**

*Shading denotes out to camera.*

Other DVC1300 series cameras may have a different pinout and would therefore not be compatible with the PCI DV 44.

\* Cable is straight through, except that wires for PSTRB + and PSTRB – are swapped.

\*\* SCNTLI and SCNTLO are single-ended RS232 signals; all others are LVDS signal pairs.

Base Configuration (with Camera Control and Serial Communication)	
Frame Grabber Connector	Channel Link Signal
1	Inner Shield
14	Inner Shield
2	X0-
15	X0+
3	X1-
16	X1+
4	X2-
17	X2+
5	Xclk-
18	Xclk+
6	X3-
19	X3+
7	SerTC+
20	SerTC-
8	SerTFG-
21	SerTFG+
9	CC1-
22	CC1+
10	CC2+
23	CC2-
23	CC2-
11	CC3-
24	CC3+
12	CC4+
25	CC4-
13	Inner Shield
26	Inner Shield

Medium and Full Configuration	
Frame Grabber Connector	Channel Link Signal
1	Inner Shield
14	Inner Shield
25	Y0-
12	Y0+
24	Y1-
11	Y1+
23	Y2-
10	Y2+
22	Yclk-
9	Yclk+
21	Y3-
8	Y3+
20	100
7	Terminated
19	Z0-
6	Z0+
18	Z1-
5	Z1+
17	Z2-
4	Z2+
4	Z2+
16	Zclk-
3	Zclk+
15	Z3-
22	Z3+
13	Inner Shield
26	Inner Shield

Table 8. PCI DV C-LINK (pdvcamlk.bit)

AIA Pin	AIA Signal	PCI RCI Signal	AIA Pin	AIA Signal	PCI RCI Signal
1	Ground	Ground	35	Ground	Ground
2	MSB+	VD0+	36	MSB-	VD0-
3	MSB1+	VD1+	37	MSB1-	VD1-
4	MSB2+	VD2+	38	MSB2-	VD2-
5	MSB3+	VD3+	39	MSB3-	VD3-
6	MSB4+	VD4+	40	MSB4-	VD4-
7	MSB5+	VD5+	41	MSB5-	VD5-
8	MSB6+	VD6+	42	MSB6-	VD6-
9	MSB7+	VD7+	43	MSB7-	VD7-
10	MSB8+	VD8+	44	MSB8-	VD8-
11	MSB9+	VD9+	45	MSB9-	VD9-
12	Ground	Ground	46	Ground	Ground
13	MSB10+	VD10+	47	MSB10-	VD10-
14	MSB11+	VD11+	48	MSB11-	VD11-
15	MSB12+	VD12+	49	MSB12-	VD12-
16	MSB13+	VD13+	50	MSB13-	VD13-
17	Do not use		51	Do not use	
18	Do not use		52	Do not use	
19	MSB14+	VD14+	53	MSB14-	VD14-
20	MSB15+	VD15+	54	MSB15-	VD15-
21	Reserved		55	Reserved	
22	Serial Control Out+	SCNTLO+	56	Serial Control Out-	SCNTLO-
23	Serial Control In+	SCNTLI+	57	Serial Control In-	SCNTLI-
24	Field ID+	FLDID+	58	Field ID-	FLDID-
25	Frame Enable+	FRME+	59	Frame Enable-	FRME-
26	Line Enable+	LINE+	60	Line Enable-	LINE-
27	Channel ID 0+	ID0+	61	Channel ID 0-	ID0-
28	Channel ID 1+	ID1+	62	Channel ID 1-	ID1-
29	Pixel Data Strobe+	PSTRB+	63	Pixel Data Strobe-	PSTRB-
30	Mode Control 0+	FRMRST/EXP+	64	Mode Control 0-	FRMRST/EXP-
31	Mode Control 1+	MC0+	65	Mode Control 1-	MC0-
32	Mode Control 2+	MC1+	66	Mode Control 2-	MC1-
33	Mode Control 3+	MC2+	67	Mode Control 3-	MC2-
34	Ground	Ground	68	Ground	Ground

**Table 9. PCI RCI for Single-Channel Grayscale Cameras (aiag\_3v.rci, aiag\_5v.rci)**

AIA Pin	AIA Signal	PCI RCI Signal	AIA Pin	AIA Signal	PCI RCI Signal
1	Ground	Ground	35	Ground	Ground
2	AMSB+	VDA0+	36	AMSB-	VDA0-
3	AMSB1+	VDA1+	37	AMSB1-	VDA1-
4	AMSB2+	VDA2+	38	AMSB2-	VDA2-
5	AMSB3+	VDA3+	39	AMSB3-	VDA3-
6	AMSB4+	VDA4+	40	AMSB4-	VDA4-
7	AMSB5+	VDA5+	41	AMSB5-	VDA5-
8	AMSB6+	VDA6+	42	AMSB6-	VDA6-
9	AMSB7+	VDA7+	43	AMSB7-	VDA7-
10	BMSB+	VDB0+	44	BMSB-	VDB0-
11	BMSB1+	VDB1+	45	BMSB1-	VDB1-
12	Ground	Ground	46	Ground	Ground
13	BMSB2+	VDB2+	47	BMSB2-	VDB2-
14	BMSB3+	VDB3+	48	BMSB3-	VDB3-
15	BMSB4+	VDB4+	49	BMSB4-	VDB4-
16	BMSB5+	VDB5+	50	BMSB5-	VDB5-
17	Do not use		51	Do not use	
18	Do not use		52	Do not use	
19	BMSB6+	VDB6+	53	BMSB6-	VDB6-
20	BMSB7+	VDB7+	54	BMSB7-	VDB7-
21	AMSB8+	BDA8+	55	AMSB8-	BDA8-
22	Serial Control Out+	SCNTLO+	56	Serial Control Out-	SCNTLO-
23	Serial Control In+	SCNTLI+	57	Serial Control In-	SCNTLI-
24	Field ID+	FLDID+	58	Field ID-	FLDID-
25	Frame Enable+	FRME+	59	Frame Enable-	FRME-
26	Line Enable+	LINE+	60	Line Enable-	LINE-
27	Channel ID 0+	ID0+	61	Channel ID 0-	ID0-
28	Channel ID 1+	ID1+	62	Channel ID 1-	ID1-
29	Pixel Data Strobe+	PSTRB+	63	Pixel Data Strobe-	PSTRB-
30	EXPOSE+	EXPOSE+	64	EXPOSE-	EXPOSE-
31	AMSB9+	VDA9+	65	AMSB9-	VDA9-
32	BMSB8+	VDB8+	66	BMSB8-	VDB8-
33	BMSB9+	VDB9+	67	BMSB9-	VDB9-
34	Ground	Ground	68	Ground	Ground

Table 10. PCI RCI for Dual-Channel Grayscale Cameras (aiag\_3v.rci, aiag\_5v.rci)

AIA Pin	AIA Signal	PCI RCI Signal	AIA Pin	AIA Signal	PCI RCI Signal
1	Ground	Ground	35	Ground	Ground
2	RedMSB0+	VDR0+	36	RedMSB0-	VDR0-
3	RedMSB1+	VDR1+	37	RedMSB1-	VDR1-
4	RedMSB2+	VDR2+	38	RedMSB2-	VDR2-
5	RedMSB3+	VDR3+	39	RedMSB3-	VDR3-
6	RedMSB4+	VDR4+	40	RedMSB4-	VDR4-
7	RedMSB5+	VDR5+	41	RedMSB5-	VDR5-
8	RedMSB6+	VDR6+	42	RedMSB6-	VDR6-
9	RedMSB7+	VDR7+	43	RedMSB7-	VDR7-
10	GrnMSB0+	VDG0+	44	GrnMSB0-	VDG0-
11	GrnMSB1+	VDG1+	45	GrnMSB1-	VDG1-
12	Ground	Ground	46	Ground	Ground
13	GrnMSB2+	VDG2+	47	GrnMSB2-	VDG2-
14	GrnMSB3+	VDG3+	48	GrnMSB3-	VDG3-
15	GrnMSB4+	VDG4+	49	GrnMSB4-	VDG4-
16	GrnMSB5+	VDG5+	50	GrnMSB5-	VDG5-
17	Do not use		51	Do not use	
18	BluMSB4+		52	BluMSB4-	
19	GrnMSB6+	VDG6+	53	GrnMSB6-	VDG6-
20	GrnMSB7+	VDG7+	54	GrnMSB7-	VDG7-
21	BluMSB0+	VDV8+	55	BluMSB0-	VDV8-
22	Serial Control Out+	SCNTLO+	56	Serial Control Out-	SCNTLO-
23	Serial Control In+	SCNTLI+	57	Serial Control In-	SCNTLI-
24	BluMSB5+	VDB5+	58	BluMSB5-	VDB5-
25	Frame Enable+	FRME+	59	Frame Enable-	FRME-
26	Line Enable+	LINE+	60	Line Enable-	LINE-
27	BluMSB6+	VDB6+	61	BluMSB6-	VDB6-
28	BluMSB7+	VDB7+	62	BluMSB7-	VDB7-
29	Pixel Data Strobe+	PSTRB+	63	Pixel Data Strobe-	PSTRB-
30	EXPOSE+	EXPOSE+	64	EXPOSE-	EXPOSE-
31	BluMSB1+	VDB1+	65	BluMSB1-	VDB1-
32	BluMSB2+	VDB2+	66	BluMSB2-	VDB2-
33	BluMSB3+	VDB3+	67	BluMSB3-	VDB3-
34	Ground	Ground	68	Ground	Ground

Table 11. PCI RCI for Single-Channel Color Cameras (aiag\_3v.rci, aiag\_5v.rci)

RCX Pin	RCX Signal	AIA Signal	RCX Pin	RCX Signal	AIA Signal
1	Ground	Ground	35	Ground	Ground
2	VD0 +	MSB +	36	VD0 –	MSB –
3	VD1 +	MSB1 +	37	VD1 –	MSB1 –
4	VD2 +	MSB2 +	38	VD2 –	MSB2 –
5	VD3 +	MSB3 +	39	VD3 –	MSB3 –
6	VD4 +	MSB4 +	40	VD4 –	MSB4 –
7	VD5 +	MSB5 +	41	VD5 –	MSB5 –
8	VD6 +	MSB6 +	42	VD6 –	MSB6 –
9	VD7 +	MSB7 +	43	VD7 –	MSB7 –
10	VD8 +	MSB8 +	44	VD8 –	MSB8 –
11	VD9 +	MSB9 +	45	VD9 –	MSB9 –
12	Spare7 +	Ground	46	Spare7 –	Ground
13	VD10 +	MSB10 +	47	VD10 –	MSB10 –
14	VD11 +	MSB11 +	48	VD11 –	MSB11 –
15	VD12 +	MSB12 +	49	VD12 –	MSB12 –
16	VD13 +	MSB13 +	50	VD13 –	MSB13 –
17	Spare17 +	Not used	51	Spare17 –	Not used
18	Spare18 +	Not used	52	Spare18 –	Not used
19	VD14 +	MSB14 +	53	VD14 –	MSB14 –
20	VD15 +	MSB15 +	54	VD15 –	MSB15 –
21	Spare16 +	Reserved	55	Spare16 –	Reserved
22	EDTIN0(RXT)	Serial Control Out 0	56	EDTIN1(RXT)	Serial Control Out 1
23	EDTOUT0(TXT)	Serial Control In 0	57	EDTOUT1(TXT)	Serial Control In 1
24	FLDID +	Field ID +	58	FLDID –	Field ID –
25	FRME +	Frame Enable +	59	FRME –	Frame Enable –
26	LINE +	Line Enable +	60	LINE –	Line Enable –
27	ID0 +	Channel ID 0 +	61	ID0 –	Channel ID 0 –
28	ID1 +	Channel ID 1 +	62	ID1 –	Channel ID 1 –
29	PSTRB +	Pixel Strobe +	63	PSTRB –	Pixel Strobe –
30	EXPOSE +	Mode Control 0 +	64	EXPOSE –	Mode Control 0 –
31	MC0 +	Mode Control 1 +	65	MC0 –	Mode Control 1 –
32	MC1 +	Mode Control 2 +	66	MC1 –	Mode Control 2 –
33	MC2 +	Mode Control 3 +	67	MC2 –	Mode Control 3 –
34	Ground	Ground	68	Ground	Ground

**Table 12. RCX Module for Single-channel Grayscale Cameras**

*Shading denotes out to camera.*

AMP	Signal	AMP	Signal
1	Ground	41	Ground
2	Ground	42	Ground
3	DATI4+	43	DATI0+
4	DATI4-	44	DATI0-
5	DATI5+	45	DATI1+
6	DATI5-	46	DATI1-
7	DATI6+	47	DATI2+
8	DATI6-	48	DATI2-
9	DATI7+	49	DATI3+
10	DATI7-	50	DATI3-
11	DATO4+	51	DATO0+
12	DATO4-	52	DATO0-
13	DATO5+	53	DATO1+
14	DATO5-	54	DATO1-
15	DATO6+	55	DATO2+
16	DATO6-	56	DATO2-
17	DATO7+	57	DATO3+
18	DATO7-	58	DATO3-
19	SPARE 0+	59	SPARE0-
20	+5V	60	+5V
21	SPARE 1+	61	SPARE1-
22	SPARE 2+	62	SPARE2-
23	Ground	63	Ground
24	STAT0+	64	RXT+
25	STAT0-	65	RXT-
26	STAT1+	66	IDV+
27	STAT1-	67	IDV-
28	STAT2+	68	DNR+
29	STAT2-	69	DNR-
30	STAT3+	70	Reserved+
31	STAT3-	71	Reserved-
32	FUNCT0+	72	SENDT+
33	FUNCT0-	73	SENDT-
34	FUNCT1+	74	ODV+
35	FUNCT1-	75	ODV-
36	FUNCT2+	76	BNR+
37	FUNCT2-	77	BNR-
38	FUNCT3+	78	TXT+
39	FUNCT3-	79	TXT-
40	Ground	80	Ground

Table 13. PCI CD (pcd8\_src.bit)

AMP	Signal	AMP	Signal
1	Ground	41	Ground
2*	Ground	42*	Ground
3	DAT4+	43	DAT0+
4	DAT4-	44	DAT0-
5	DAT5+	45	DAT1+
6	DAT5-	46	DAT1-
7	DAT6+	47	DAT2+
8	DAT6-	48	DAT2-
9	DAT7+	49	DAT3+
10	DAT7-	50	DAT3-
11	DAT12+	51	DAT8+
12	DAT12-	52	DAT8-
13	DAT13+	53	DAT9+
14	DAT13-	54	DAT9-
15	DAT14+	55	DAT10+
16	DAT14-	56	DAT10-
17	DAT15+	57	DAT11+
18	DAT15-	58	DAT11-
19	SPARE 0+	59	SPARE0-
20	+5V	60	+5V
21	SPARE 1+	61	SPARE1-
22	SPARE 2+	62	SPARE2-
23	Ground	63	Ground
24	STAT0+	64	RXT+
25	STAT0-	65	RXT-
26	STAT1+	66	IDV+
27	STAT1-	67	IDV-
28	STAT2+	68	DNR+
29	STAT2-	69	DNR-
30	STAT3+	70	Reserved+
31	STAT3-	71	Reserved-
32	FUNCT0+	72	SENDT+
33	FUNCT0-	73	SENDT-
34	FUNCT1+	74	ODV+
35	FUNCT1-	75	ODV-
36	FUNCT2+	76	BNR+
37	FUNCT2-	77	BNR-
38	FUNCT3+	78	TXT+
39	FUNCT3-	79	TXT-
40	Ground	80	Ground

**Table 14. PCI CD and PCI CDa (pcd\_src.bit, pcd\_looped.bit, pcda.bit)**

\*On PCI CDa, these pins are Spare.

P3	Channel-Pin	Signal	P3	Channel-Pin	Signal
1	CH1-25	Ground	41	CH2-25	Ground
2	CH1-25	Ground	42	CH2-25	Ground
3	CH2-3	CH2D0+	43	CH1-3	CH1D0+
4	CH2-4	CH2D0-	44	CH1-4	CH1D0-
5	CH2-5	CH2D1+	45	CH1-5	CH1D1+
6	CH2-6	CH2D1-	46	CH1-6	CH1D1-
7	CH2-7	CH2D2+	47	CH1-7	CH1D2+
8	CH2-8	CH2D2-	48	CH1-8	CH1D2-
9	CH2-9	CH2D3+	49	CH1-9	CH1D3+
10	CH2-10	CH2D3-	50	CH1-10	CH1D3-
11	CH4-3	CH4D0+	51	CH3-3	CH3D0+
12	CH4-4	CH4D0-	52	CH3-4	CH3D0-
13	CH4-5	CH4D1+	53	CH3-5	CH3D1+
14	CH4-6	CH4D1-	54	CH3-6	CH3D1-
15	CH4-7	CH4D2+	55	CH3-7	CH3D2+
16	CH4-8	CH4D2-	56	CH3-8	CH3D2-
17	CH4-9	CH4D3+	57	CH3-9	CH3D3+
18	CH4-10	CH4D3-	58	CH3-10	CH3D3-
19		Not used	59		Not used
20		5V DC (fused)	60		5V DC (fused)
21		Not used	61		Not used
22		Not used	62		Not used
23	CH3-25	Ground	63	CH4-25	Ground
24		Reserved	64	CH1-1	CH1CLK+
25		Reserved	65	CH1-2	CH1CLK-
26		Reserved	66		Reserved
27		Reserved	67		Reserved
28		Reserved	68		Reserved
29		Reserved	69		Reserved
30		Reserved	70	CH3-1	CH3CLK+
31		Reserved	71	CH3-2	CH3CLK-
32	CH2-1	CH2CLK+	72		Reserved
33	CH2-2	CH2CLK-	73		Reserved
34		Reserved	74		Reserved
35		Reserved	75		Reserved
36		Reserved	76		Reserved
37		Reserved	77		Reserved
38	CH4-1	CH4CLK+	78		Reserved
39	CH4-2	CH4CLK-	79		Reserved
40	CH3-25	Ground	80	CH4-25	Ground

Table 15. PCI CD (ssd.bit, ssd2.bit, ssd4.bit)

EDT Pinouts

P3	Channel-Pin	Signal	P3	Channel-Pin	Signal
1	CH1-25	Ground	41	CH2-25	Ground
2	CH1-25	Ground	42	CH2-25	Ground
3	CH2-3	CH2D0+	43	CH1-3	CH1D0+
4	CH2-4	CH2D0-	44	CH1-4	CH1D0-
5	CH2-5	CH2D1+	45	CH1-5	CH1D1+
6	CH2-6	CH2D1-	46	CH1-6	CH1D1-
7	CH2-7	CH2D2+	47	CH1-7	CH1D2+
8	CH2-8	CH2D2-	48	CH1-8	CH1D2-
9	CH2-9	CH2D3+	49	CH1-9	CH1D3+
10	CH2-10	CH2D3-	50	CH1-10	CH1D3-
11	CH4-3	CH4D0+	51	CH3-3	CH3D0+
12	CH4-4	CH4D0-	52	CH3-4	CH3D0-
13	CH4-5	CH4D1+	53	CH3-5	CH3D1+
14	CH4-6	CH4D1-	54	CH3-6	CH3D1-
15	CH4-7	CH4D2+	55	CH3-7	CH3D2+
16	CH4-8	CH4D2-	56	CH3-8	CH3D2-
17	CH4-9	CH4D3+	57	CH3-9	CH3D3+
18	CH4-10	CH4D3-	58	CH3-10	CH3D3-
19		Not used	59		Not used
20		5V DC (fused)	60		5V DC (fused)
21		Not used	61		Not used
22		Not used	62		Not used
23	CH3-25	Ground	63	CH4-25	Ground
24		Reserved	64	CH1-1	CH1CLK+
25		Reserved	65	CH1-2	CH1CLK-
26		Reserved	66		Reserved
27		Reserved	67		Reserved
28		Reserved	68		Reserved
29		Reserved	69		Reserved
30		Reserved	70	CH3-1	CH3CLK+
31		Reserved	71	CH3-2	CH3CLK-
32	CH2-1	CH2CLK+	72		Reserved
33	CH2-2	CH2CLK-	73		Reserved
34		Reserved	74		Reserved
35		Reserved	75		Reserved
36		Reserved	76		Reserved
37		Reserved	77		Reserved
38	CH4-1	CH4CLK+	78		Reserved
39	CH4-2	CH4CLK-	79		Reserved
40	CH3-25	Ground	80	CH4-25	Ground

Table 16. PCI CD (ssdout1.bit, ssdio.bit, ssdio\_neg.bit)



P3	Channel-Pin	P3	Channel-Pin
1	Ground	41	Ground
2	Ground	42	Ground
3	CH2D+	43	CH0D+
4	CH2D-	44	CH0D-
5	CH2CLK+	45	CH0CLK+
6	CH2CLK-	46	CH0CLK-
7	CH3D+	47	CH1D+
8	CH3D-	48	CH1D-
9	CH3CLK+	49	CH1CLK+
10	CH3CLK-	50	CH1CLK-
11	CH6D+	51	CH4D+
12	CH6D-	52	CH4D-
13	CH6CLK+	53	CH4CLK+
14	CH6CLK-	54	CH4CLK-
15	CH7D+	55	CH5D+
16	CH7D-	56	CH5D-
17	CH7CLK+	57	CH5CLK+
18	CH7CLK-	58	CH5CLK-
19	EXTCLKIN+	59	EXTCLKIN-
20	+5V	60	+5V
21	Spare	61	Spare
22	Spare	62	Spare
23	Spare	63	Spare
24	CH8D+	64	CH10D+
25	CH8D-	65	CH10D-
26	CH8CLK+	66	CH10CLK+
27	CH8CLK-	67	CH10CLK-
28	CH9D+	68	CH11D+
29	CH9D-	69	CH11D-
30	CH9CLK+	70	CH11CLK+
31	CH9CLK-	71	CH11CLK-
32	CH12D+	72	CH14D+
33	CH12D-	73	CH14D-
34	CH12CLK+	74	CH14CLK+
35	CH12CLK-	75	CH14CLK-
36	CH13D+	76	CH15D+
37	CH13D-	77	CH15D-
38	CH13CLK+	78	CH15CLK+
39	CH13CLK-	79	CH15CLK-
40	GROUND	80	GROUND

Table 17. PCI CDa (ssd16io.bit)

## EDT Pinouts

AMP	Signal	AMP	Signal
1	TXT+	35	TXT-
2	DATI0+	36	DATI0-
3	DATI1+	37	DATI1-
4	DATI2+	38	DATI2-
5	DATI3+	39	DATI3-
6	DATI4+	40	DATI4-
7	DATI5+	41	DATI5-
8	DATI6+	42	DATI6-
9	DATI7+	43	DATI7-
10	DATO0+	44	DATO0-
11	DATO1+	45	DATO1-
12	STAT3+	46	STAT3-
13	DATO2+	47	DATO2-
14	DATO3+	48	DATO3-
15	DATO4+	49	DATO4-
16	DATO5+	50	DATO5-
17	FUNCT1+	51	FUNCT1-
18	FUNCT2+	52	FUNCT2-
19	DATO6+	53	DATO6-
20	DATO7+	54	DATO7-
21	SPARE0+	55	SPARE0-
22	STAT0+	56	STAT0-
23	FUNCT0+	57	FUNCT0-
24	Reserved	58	Reserved
25	DNR+	59	DNR-
26	IDV+	60	IDV-
27	STAT1+	61	STAT1-
28	STAT2+	62	STAT2-
29	RXT+	63	RXT-
30	FUNCT3+	64	FUNCT3-
31	SENDT+	65	SENDT-
32	ODV+	66	ODV-
33	BNR+	67	BNR-
34	Ground	68	Ground

Table 18. PCI GP (gp\_pcd8.bit)

AMP	Signal	AMP	Signal
1	TXT+	35	TXT-
2	DAT0+	36	DAT0-
3	DAT1+	37	DAT1-
4	DAT2+	38	DAT2-
5	DAT3+	39	DAT3-
6	DAT4+	40	DAT4-
7	DAT5+	41	DAT5-
8	DAT6+	42	DAT6-
9	DAT7+	43	DAT7-
10	DAT8+	44	DAT8-
11	DAT9+	45	DAT9-
12	STAT3+	46	STAT3-
13	DAT10+	47	DAT10-
14	DAT11+	48	DAT11-
15	DAT12+	49	DAT12-
16	DAT13+	50	DAT13-
17	FUNCT1+	51	FUNCT-
18	FUNCT2+	52	FUNCT2-
19	DAT14+	53	DAT14-
20	DAT15+	54	DAT15-
21	SPARE0+	55	SPARE0-
22	STAT0+	56	STAT0-
23	FUNCT0+	57	FUNCT0-
24	Reserved	58	Reserved
25	DNR+	59	DNR-
26	IDV+	60	IDV-
27	STAT1+	61	STAT1-
28	STAT2+	62	STAT2-
29	RXT+	63	RXT-
30	FUNCT3+	64	FUNCT3-
31	SENDT+	65	SENDT-
32	ODV+	66	ODV-
33	BNR+	67	BNR-
34	Ground	68	Ground

Table 19. PCI GP (gp\_pcd.bit) and PCI SS (ss\_pcd.bit)

## EDT Pinouts

AMP	Signal	AMP	Signal
1	Reserved	35	Reserved
2	CH1D0+	36	CH1D0-
3	CH1D1+	37	CH1D1-
4	CH1D2+	38	CH1D2-
5	CH1D3+	39	CH1D3-
6	CH2D0+	40	CH2D0-
7	CH2D1+	41	CH2D1-
8	CH2D2+	42	CH2D2-
9	CH2D3+	43	CH2D3-
10	CH3D0+	44	CH3D0-
11	CH3D1+	45	CH3D1-
12	Reserved	46	Reserved
13	CH3D2+	47	CH3D2-
14	CH3D3+	48	CH3D3-
15	CH4D0+	49	CH4D0-
16	CH4D1+	50	CH4D1-
17	Reserved	51	Reserved
18	Reserved	52	Reserved
19	CH4D2+	53	CH4D2-
20	CH4D3+	54	CH4D3-
21	Reserved	55	Reserved
22	Reserved	56	Reserved
23	CH2CLK+	57	CH2CLK-
24	CH3CLK+	58	CH3CLK-
25	Reserved	59	Reserved
26	Reserved	60	Reserved
27	Reserved	61	Reserved
28	Reserved	62	Reserved
29	CH1CLK+	63	CH1CLK-
30	CH4CLK+	64	CH4CLK-
31	Reserved	65	Reserved
32	Reserved	66	Reserved
33	Reserved	67	Reserved
34	Ground	68	Ground

**Table 20. PCI GP (gpssd4.bit)**

## EDT Pinouts

Channel-Pin	AMP	Signal	Wire Color Code	Channel-Pin	AMP	Signal	Wire Color Code
	1	Not used			35	Not used	
CH0-3	2	CH0D0+	Br-Tan	CH0-4	36	CH0D0-	Tan-Br
CH0-1	3	CH0CLK+	Br-W	CH0-2	37	CH0CLK-	W-Br
	4	Not used			38	Not used	
	5	Not used			39	Not used	
	6	Not used			40	Not used	
	7	Not used			41	Not used	
	8	Not used			42	Not used	
	9	Not used			43	Not used	
CH1-3	10	CH1D0+	Grn-Tan	CH1-4	44	CH1D0-	Tan-Grn
CH1-1	11	CH1CLK+	Pink-W	CH1-2	45	CH1CLK-	W-Pink
	12	Not used			46	Not used	
	13	Not used			47	Not used	
	14	Not used			48	Not used	
	15	Not used			49	Not used	
	16	Not used			50	Not used	
	17	Not used			51	Not used	
	18	Not used			52	Not used	
	19	Not used			53	Not used	
	20	Not used			54	Not used	
	21	Not used			55	Not used	
	22	Not used			56	Not used	
	23	Not used			57	Not used	
	24	Not used			58	Not used	
	25	Not used			59	Not used	
CH2-1	26	CH2CLK+	W-Or	CH2-2	60	CH2CLK-	Or-W
	27	Not used			61	Not used	
	28	Not used			62	Not used	
CH2-3	29	CH2D0+	Pink-Br	CH2-4	63	CH2D0-	Br-Pink
	30	Not used			64	Not used	
CH3-3	31	CH3D0+	Bl-Br	CH3-4	65	CH3D0-	Br-Bl
YCH3-1	32	CH3CLK+	Grn-W	CH3-2	66	CH3CLK-	W-Grn
	33	Not used			67	Not used	
CH0-5	34	*Ground	Tan-Yel	CH2-5	68	*Ground	Yel-W
CH1-5	34	*Ground	Yel-Tan	CH3-5	68	*Ground	W-Yel

**Table 21. PCI GP (ssd4io.bit)**

\* These connections share ground wire from 68-position connector.

AMP	Signal	AMP	Signal
1	CH15CLK+	35	CH15CLK-
2	CH0D+	36	CH0D-
3	CH0CLK+	37	CH0CLK-
4	CH1D+	38	CH1D-
5	CH1CLK+	39	CH1CLK-
6	CH2D+	40	CH2D-
7	CH2CLK+	41	CH2CLK-
8	CH3D+	42	CH3D-
9	CH3CLK+	43	CH3CLK-
10	CH4D+	44	CH4D-
11	CH4CLK+	45	CH4CLK-
12	CH9CLK+	46	CH9CLK-
13	CH5D+	47	CH5D-
14	CH5CLK+	48	CH5CLK-
15	CH6D+	49	CH6D-
16	CH6CLK+	50	CH6CLK-
17	CH12CLK+	51	CH12CLK-
18	CH13D+	52	CH13D-
19	CH7D+	53	CH7D-
20	CH7CLK+	54	CH7CLK-
21	EXTIN+	55	EXTIN-
22	CH8D+	56	CH8D-
23	CH12D+	57	CH12D-
24	CH11CLK+	58	CH11CLK-
25	CH11D+	59	CH11D-
26	CH10CLK+	60	CH10CLK-
27	CH8CLK+	61	CH8CLK-
28	CH9D+	62	CH9D-
29	CH10D+	63	CH10D-
30	CH13CLK+	64	CH13CLK-
31	CH14D+	65	CH14D-
32	CH14CLK+	66	CH14CLK-
33	CH15D+	67	CH15D-
34	Ground	68	Ground

Table 22. PCI GP (ssd16.bit, ssd16in.bit, eclssd16in.bit)

DB9A	DB9B	Signal
1	1	Reserved
2	2	Ground
3	3	Reserved
4	4	Ground
5	5	Reserved
6	6	DAT-
7	7	DAT+
8	8	CLK-
9	9	CLK+

**Table 23. PCI GP SSE (pcdssd.bit)**

## EDT Pinouts

Positive Pin #	Negative Pin #	Signal Type	E1 or T1 Channel #		Function
			Input	Output	
1	35	E1 or T1	0	8	
2	36	Differential I/O			DATA1
3	37	Differential I/O			DATA7
4	38	Differential I/O			CLK1
5	39	E1 or T1	1	9	
6	40	Differential I/O			DATA2
7	41	Differential I/O			CLOCK7
8	42	Differential I/O			CLK2
9	43	E1 or T1	3	11	
10	44	Differential I/O			DATA3
11	45	Differential I/O			DATA8
12	46	E1 or T1	9	1	
13	47	Differential I/O			CLK3
14	48	E1 or T1	5	13	
15	49	Differential I/O			DATA4
16	50	Differential I/O			CLOCK8
17	51	E1 or T1	12	4	
18	52	E1 or T1	4	12	
19	53	Differential I/O			CLK4
20	54	E1 or T1	7	15	
21	55	LVDS Differential Input			none
22	56	Differential I/O			DATA5
23	57	E1 or T1	2	10	
24	58	E1 or T1	11	3	
25	59	Differential I/O			CLOCK6
26	60	E1 or T1	10	2	
27	61	E1 or T1	8	0	
28	62	Differential I/O			CLK5
29	63	Differential I/O			DATA6
30	64	E1 or T1	13	5	
31	65	E1 or T1	6	14	
32	66	E1 or T1	14	6	
33	67	E1 or T1	15	7	
34	68	Ground			Ground

**Table 24. PCI SS Combo (combo16in.bit)**

## EDT Pinouts

Positive Pin #	Negative Pin #	Signal Type	E3 or T3 Channel #	
			Input	Output
1	2	E3 or T3	0	2
3	4	E3 or T3	1	3
5	6	E3 or T3	2	0
7	8	E3 or T3	3	1
9	11	Ground		
13	15	Ground		

**Table 25. PCI SS Combo (combo16in.bit)**

EDT Pinouts

AMP	STD P1	DEC P1	Signal		DEC P2	STD P2	AMP
1	1	VV	DO15	DI15	VV	1	41
2	2	UU	DO00	DI00	UU	2	42
3	3	TT	DO14	DI14	TT	3	43
4	4	SS	DO01	DI01	SS	4	44
5	5	RR	DO13	DI13	RR	5	45
6	6	PP	DO02	DI02	PP	6	46
7	7	NN	DO12	DI12	NN	7	47
8	8	MM	DO03	DI03	MM	8	48
9	9	LL	DO11	DI11	LL	9	49
10	10	KK	DO04	DI04	KK	10	50
11	11	JJ	DO10	DI10	JJ	11	51
12	12	HH	DO05	DI05	HH	12	52
13	13	FF	DO09	DI09	FF	13	53
14	14	EE	DO06	DI06	EE	14	54
15	15	DD	DO08	DI08	DD	15	55
16	16	CC	DO07	DI07	CC	16	56
17	17	BB	NC	NC	BB	17	57
18	18	AA	GROUND	GROUND	AA	18	58
19	19	Z	CYCRQ B	GROUND	Z	19	59
20	20	Y	GROUND	GROUND	Y	20	60
21	21	X	END CYCLE	GO H	X	21	61
22	22	W	GROUND	GROUND	W	22	62
23	23	V	STATUS C	FNCT1	V	23	63
24	24	U	GROUND	GROUND	U	24	64
25	25	T	STATUS C	C1 CNTROL	T	25	65
26	26	S	GROUND	GROUND	S	26	66
27	27	R	STATUS B	FNCT2	R	27	67
28	28	P	GROUND	GROUND	P	28	68
29	29	N	INIT	C0 CNTRL	N	29	69
30	30	M	GROUND	GROUND	M	30	70
31	31	L	STATUS A	FNCT3	L	31	71
32	32	K	BURST RQ	FNCT3	K	32	72
33	33	J	WC INC ENB	BC INC ENB	J	33	73
34	34	H	GROUND	GROUND	H	34	74
35	35	F	READY	A00	F	35	75
36	36	E	GROUND	GROUND	E	36	76
37	37	D	ACLO FNCT2	ATTN	D	37	77
38	38	C	GROUND	GROUND	C	38	78
39	39	B	CYCRQ A	BUSY	B	39	79
40	40	A	GROUND	GROUND	A	40	80

Table 26. PCI 11W (p11w\_3v.bit, p11w\_5v.bit)

## EDT Pinouts

AMP	STD P1	Signal	AMP	STD P2	Signal
1	1	DO15	41	1	DI15
2	2	DO00	42	2	DI00
3	3	DO14	43	3	DI14
4	4	DO01	44	4	DI01
5	5	DO13	45	5	DI13
6	6	DO02	46	6	DI02
7	7	DO12	47	7	DI12
8	8	DO03	48	8	DI03
9	9	DO11	49	9	DI11
10	10	DO04	50	10	DI04
11	11	DO10	51	11	DI10
12	12	DO05	52	12	DI05
13	13	DO09	53	13	DI09
14	14	DO06	54	14	DI06
15	15	DO08	55	15	DI08
16	16	DO07	56	16	DI07
17	17	GROUND	57	17	NC
18	18	GROUND	58	18	GROUND
19	19	RSVD IN	59	19	GROUND
20	20	GROUND	60	20	GROUND
21	21	RDSTRBL	61	21	OUTVALIDL
22	22	GROUND	62	22	GROUND
23	23	STAUS C	63	23	FNCT0
24	24	GROUND	64	24	GROUND
25	25	STATUS C	65	25	RSVD IN
26	26	GROUND	66	26	GROUND
27	27	STATUS B	67	27	FNCT1
28	28	GROUND	68	28	GROUND
29	29	DEVINIT L	69	29	RSVD IN
30	30	GROUND	70	30	GROUND
31	31	STATUS A	71	31	FNCT2
32	32	NC	72	32	FNCT2
33	33	RSVD IN	73	33	RSVD IN
34	34	GROUND	74	34	GROUND
35	35	SDMAEN L	75	35	RSVD IN
36	36	GROUND	76	36	GROUND
37	37	DMAINPUT L	77	37	DEVINT L
38	38	GROUND	78	38	GROUND
39	39	DCLKL P	79	39	DACK P
40	40	GROUND	80	40	GROUND

Table 27. PCI 16D (p16d\_3v.bit, p16d\_5v.bit)

## EDT Pinouts

Pin	Signal	Description
1	VCC	Output, fused 5V for external transceivers, maximum 500 mA
2	RXD	Serial debug port input from onboard SPARC, Channel A RS-232 receive
3	TXD	Serial debug port output from onboard SPARC, Channel A RS-232 transmit
4	IRIG B	Input, analog time signal from GPS, to synchronize time-base counters among multiple PCI53B boards (independent of an IRIG B time source)
5	GND	Logic ground
6	SYNC+	in/out, RS-422 differential pair to synchronize time-base counters among multiple PCI53B boards (independent of an IRIG B time source)
7	SYNC-	
8	SPARE+	Input, RS-422 differential pair
9	SPARE-	

**Table 28. PCI 53B (xc21b.blk)**